Market-leading Hardware/Software Co-Verification
Seamless for Field Programmable SoC

- FPSoC devices share many of the same challenges of the SoC and Board methodologies they will replace:
  - **Hardware & Software** - must be developed and verified together
  - **Controllability & Observability** - gaining access to all the signal & processor information, pre-silicon & post silicon playback
  - **Early Availability** - designing 1M+ gates is a lengthy process - how soon can you start software debug?
  - **System Considerations** - most systems will contain devices (memories, co-processors, etc) outside the FPSoC
Hardware/Software Co-Verification

Seamless Hardware/Software Co-Verification provides a Virtual Prototyping environment that enables early, productive debug of complex embedded systems.

- Early Availability
- Controllability
  - stop clock
  - single step
  - “what if?” analysis
- Observability
  - all signals, all internals available
- Ease of change
- Ease of debug
- Performance profiling
Virtual Prototyping: Logic Simulation

- Logic simulation can:
  - show how hardware responds to software
  - model interrupts, resets, other events that effect software
  - show how hardware timing can impact software execution
  - give access and trace of any signal or node in the design
  - allow ‘what if’ analysis of hardware events

- Simulation can not:
  - give visibility of processor or memory internals
  - show ‘C’ or assembly code
  - show how software responds to hardware stimuli
  - simulate sufficient code
Virtual Prototyping: Software Simulation

- Software (Instruction Set) Simulation can:
  - view code, registers, memory
  - step through code
  - show how software reacts to hardware

- Software Simulation can not:
  - model clocks
  - model external hardware
  - model interrupts, exceptions, resets
  - show bus contention, protocol violations, timing issues
Virtual Prototyping: Hardware/Software Co-Verification

Combining software + hardware simulation gives all the benefits & removes restrictions
Debug/Flow Control in Co-Verification

- Controls the flow of data from ISS to Logic Simulator (& back)
- Without optimizations, all cycles are routed through logic simulator
- Full debug of all logic & software events
- Can drive both environments from single location
Optimizing Co-Verification Performance

- **“Instruction Fetch & Memory Access” Optimization**
- **Some or all memory accesses routed direct to memory server**
  - User specifies which and when
- **Clock cycles driven to logic simulator**
Optimizing Co-Verification Performance

- **“Time” Optimization**
- **Some or all memory accesses routed direct to memory server**
  - User specifies which and when
- **Clock cycles NOT driven to logic simulator**
Optimizing Co-Verification Performance

- Optimization Controlling
  - Through the Seamless GUI
    - switch optimizations on/off
    - define optimization ‘recipes’
  - Through the Logic Simulator
    - associate Seamless commands with hardware events
  - Through the Debugger
    - associate Seamless commands with software states or events
Seamless with Excalibur: Current Status

- Get the Stripe Netlist for Seamless:
  - Insert ARM922T PSP
  - Use Seamless Compatible Memories
- Create Seamless Configuration File
  - Describe to Seamless how to invoke the ISS & load the software
  - Define the memory map & configuration
- Run Co-Verification
Seamless with Excalibur: Solution

“Super PSP” Delivery from Mentor Graphics including:

- Excalibur stripe netlist ready to use with Seamless:
  - ARM922T PSP
  - Seamless-ized memory models
- Scripts to read configuration registers to automatically generate Seamless Configuration File
Seamless ARM922 PSP

- ARM922t r0 == ARM920t r1 with 8KB I/D Caches
- Based on high-performance, cycle accurate co-verification Model from ARM
- Supports XRAY, ADU and ARMSD debuggers
- Interface to ModelSIM, and all popular Verilog and VHDL simulators
- Integrated with 3rd party tools (e.g. Verisity SpecMan Elite)

Instruction Set Simulator (ISS)
- Complete instruction set
- Registers
- InterruptReset
- Instruction Timing

Coherent Memory Server

VHDL/Verilog Pin Wrapper

BUS Interface Model (BIM)
- Peripherals
- Bus Cycle Timing
- Controllers (DMA, MMU, Cache …)
Mentor Graphics continues to be the leading supplier of ARM processor co-verification models

- ARM7™ Family
- ARM9™ Family
- ARM9E™ Family
- ARM10™ Family
- ARM Jazelle Technology™ Family
Seamless with C-Bridge

- Extend co-verification to reach C-based prototyping and accelerated verification
  - Support for integration of ‘C’ models
  - Enables rapid prototyping of functionality & performance
  - Earlier verification at higher abstraction
  - Single language to refine into either HW or SW

- Provide API to support all popular dialects of C
  - Anything that exposes a C interface and whose interface can be expressed in a dataflow, cycle or event semantics
  - Support ANSI C, SystemC and CynLib models
Seamless With C-Bridge

Application SW

- ‘C’ HW .dll
- C-Bridge Bus Access API
- New HW Abstract ‘C’ Bus Peripheral

C Host Code Debug

Pins

HDL Design

- CPU Core
- DSP Core
- New HW IP
- Mem Cont.
- CPU Perif.
- Glue Logic
- Memory
- I/O

- No changes to HDL or SW code
- Use C-Bridge API to interface C model into design
- Load C HW dynamic library from Seamless configuration file
- Optional connection of control pins
Seamless Co-Verification Summary

- Virtual Prototyping
  - provides a flexible, controllable environment for the design and debug of complex systems

- Seamless Hardware/Software Co-Verification
  - links together hardware and software simulation environments into an effective Virtual Prototype

- Seamless / Excalibur Integration
  - allows Excalibur users to rapidly create Seamless configuration file and to focus on the validation of their original SW against their original HW
For More Product Information

- [www.mentor.com/seamless](http://www.mentor.com/seamless)
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