Seamless delivers high-performance, high validity co-verification for both Altera Excalibur system-on-a-programmable-chip (SOPC) solutions and the systems that utilize them, reducing the risk of integration errors and improving time-to-market.

Seamless with Excalibur Solutions

The Seamless solution for Altera SOPC solutions provides a complete co-verification ready model of the Excalibur stripe that includes an ARM922T processor.

Key product features

- Cycle-accurate Seamless® ARM922T PSP and Seamless software for Altera® Excalibur™ Processor Solutions
- Seamless ready models for Altera SRAM and DPRAM stripe memories
- Full visibility and control of hardware and software execution
- Dynamic performance optimizations
- Easy to use – no hardware or software changes required
- Single point of control for hardware and software simulation
- Supports all popular VHDL and Verilog simulators including ModelSim®
- C-Bridge™ interface for integration of C/C++ modules

Seamless Hardware/Software Co-Verification for Excalibur Embedded Processor Solutions

Seamless Co-Verification Excalibur Processor Solutions

www.mentor.com/seamless
Seamless and Excalibur Devices

Mentor Graphics and Altera have partnered to create a high-performance, high-accuracy co-verification solution for the Excalibur family of SOPC devices. Starting with the industry-leading Seamless software and the cycle-accurate ARM922T Seamless processor support package (PSP), a solution tailored to the needs of engineers designing with Excalibur devices has been created.

The Seamless solution for Excalibur devices enables the concurrent verification of hardware and software in both the Excalibur devices and the systems that use them. Verification is on a virtual prototype of the device or system weeks or months before physical prototypes are available. Using virtual prototypes provides levels of controllability, observability, and analysis that are difficult or impossible to achieve with physical hardware.

Performance Optimization: the Key to Efficient Co-Verification

Seamless supports Dynamic Optimizations, a set of options which, under user control, routes memory requests from the ISS to the Coherent Memory Server, either directly, or via the logic simulator.

Utilizing optimizations allows the designer to switch between high-performance (direct access) and high-validity simulation as dictated by the system architecture and debug requirements.

Seamless optimizations give you the ultimate in resolution, allowing the freedom to choose which areas of memory are optimized, and when they are optimized — all without the need to halt or restart simulation.

The Coherent Memory Server supports multi-processor designs and processors with multiple address spaces and a wide range of commonly used memory management techniques such as interleaving, remapping, error code correction, and parity checking.

Embedded Software Capability

Seamless is designed to simulate hardware/software interactions. Software functionality typically run on Seamless includes:
- Boot code
- Hardware diagnostics
- Device drivers
- RTOS

In addition, Seamless can run application code. There is no hard limit to the size of application, however simulation run-time becomes a practical limit for large applications.

The patented Seamless Coherent Memory Server empowers you to switch dynamically between detailed hardware verification and high-speed software execution.

Visit our web site at www.mentor.com/seamless for the latest product news.