New Approaches to Mixed-Signal Testing and Design-For-Test

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Outline

• Industry Trends
• Technology Trends
  - SOC Designs and Emerging Failure Mechanisms
  - Failure and Yield Analysis Challenges
  - Technology Scaling and the Cost of Test
• Overview of BIST
• Mixed-Signal BIST Methods
• Summary
Fabless Revenue Growth vs. the Semiconductor Industry
The Rise of Subcontract Manufacturing

• The Growth of Foundry Market Share
  - Foundry market share to grow from 12.5% in 2000 to 19.4% in 2004 (in units produced).
  - Foundry market share expected to reach 25-40% by 2010.
  - 30-40% of new fabs are foundry fabs.

• Fabless Semiconductor Growth
  - Fabless companies, driven by communications, growing at 30-40%, more than double the industry rate (15%).
  - Over 65 public fabless companies produced $16 billion in revenue in 2000, over 9% of total ($170 billion), up from less than 5% in 1995.
  - IDMs are also becoming “fabless”: Motorola to outsource 50%, Lucent to go from 13% foundry in 1999 to 30% in 2001, Toshiba to go from 7% to 25% by 2002-2003.
The Disaggregated Semiconductor Value Chain
Who Owns IC Yield, Quality, and Reliability?

• Library & IP Providers?
  - Frequently testability is not considered

• Design?
  - More than 50% of design effort involves verification
  - Deep submicron processes involve larger numbers of unsimulatable features, which increases manufacturing risk
  - Adding testability features increases design time, which may impact tapeout dates

• Fab?
  - Most aware of causes of failure but not the design
  - Increased design-process interdependencies require design-specific process adjustments by the fab
Test Engineers Discover Issues Relating to Yield, Quality, and Reliability First

- Test programs need to be capable of detecting and diagnosing all problems at low cost and with minimal test time.
- Root cause analysis may be limited by the availability of design-of-test features.
- The fab will try to hide problems
  - High defect densities are not detectable with data from the scribe line
  - Scribe lines may not include all relevant test structures
- Test programs have incomplete fault coverage
  - 8% of chips are marginal, i.e. include resistive defects, electromigration induced failures at contact interfaces, oxide failures which are activated by stress
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System-On-Chip Designs are Increasing

- Technology scaling has enabled the design of larger and more complex chips
  - Chip sets are being designed as single chips
- Emerging technology requirements
  - Mixed Signal, RF, embedded DRAM, embedded flash, etc. integrated with higher performance digital technologies.
- New Failure Mechanisms
  - Do we need to modify our approach to structured test?
  - Can there be a mixed-signal fault model?
Evolution of Defects

• In the 1970’s most defects were caused by air particles which impacted the photolithographic process
• In the 1980’s the dominant source of defects became the manufacturing equipment
• Today more and more defects are non-visible, i.e. process variations, particles blocking implant, device mismatch, tiny particles causing oxide breakdown
Emerging Failure Mechanisms – Chemical Mechanical Polishing Uniformity

• Polishing of copper depends on the local density of the mask
• Areas with high density will have higher coupling capacitances between copper lines
Emerging Failure Mechanisms – Within-Chip Gate CD Variation

- Lens aberrations in lithography cause systematic variation in the gate CD
- Gate CD variation results in clock skew
Emerging Challenges in Failure Analysis

- The Traditional Approach to Failure Analysis involves the use of photo-emission analysis and liquid-crystal techniques
- Photo-emission analysis and liquid-crystal techniques are becoming obsolete for efficient fault isolation because of:
  - Decreasing supply voltages and feature sizes
  - Increasing metal coverage and circuit complexity, reducing the traceability of signals, especially in the absence of design-for-test (DFT)!
Emerging Challenges in Yield Analysis

- The Traditional Approach to Yield Analysis involves correlating sort yield to test structure parameters from the scribe line, aggregating data by wafer.
- Correlations between test structure parameters from the scribe line and sort yield are less effective for efficient identification of product-process sensitivities because of:
  - Increasing wafer size and process variation across the wafer and reticle field.
  - Increasing process complexity requiring more test structures for monitoring.
  - Increasing impact of design density on feature formation, i.e. the chip may be different than the scribe line!
The Result of Inefficient Approaches to Failure Analysis and Yield Analysis

- **Delays in Bringing Products to Market**
  - Products become obsolete prior to introduction
  - The average selling price falls below expectations due to competition from other vendors
- **Delays in identifying yield detractors**
  - Higher manufacturing cost
- **50% of prototypes never go into production!**
Example of a Product Produced with High Manufacturing Cost

Yield Histogram for the Same Product in Two Fabs

- The problem with Fab 1 could not be detected by analysis to the test structure data on the scribe lines
- What if Fab 2 data were not available?
Impact of Technology Scaling on the Cost of Test

- Manufacturing cost has been reduced by approximately 30% for each technology generation
- Testing cost has remained constant
- Over several technology generations, the cost of test will approach the cost of manufacturing!
The Cost of Test Problem

- Tester speeds have not kept pace with chip speeds
  - Tester timing margins are a significant fraction of chip cycle times
- The industry is increasingly turning to Built-In Self Test (BIST) and Low Cost Testers to address the Cost of Test Problem
- However, in order to move to a Low Cost Tester, BIST is required for ALL components of the SOC.
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Two Purposes of BIST

- Reduction of Production Cost Through Building Test Circuitry On Chip
- Checking of Long-Term Reliability Through Periodic Self-Checking Of Chip Performance

Issues
- Area overhead
- Power consumption
- Performance degradation
- Additional design effort
- Compatibility with existing test approaches
**BIST Methods**

- SOCs combine diverse functionality, including:
  - Digital Logic
  - Memory
  - Analog

- Commercial BIST Solutions are available for Digital Logic and Memory

- Solutions for Mixed-Signal BIST are Emerging, but BIST is not widely accepted by the Mixed-Signal Community

- Why?
  - Performance degradation, area overhead, additional design effort, confidence in the test results, etc.
Challenges for Mixed-Signal Testing

- Lack of a Structured Test Methodology
- Lack of an “accepted” Analog Fault Model
- Advanced Processes Change Rapidly, i.e. Process are Not Stable
  - Difficult to obtain good process characterization data
  - Simulation-based results are not well accepted
The Analog Fault Model (as of Today)

• Fault Characterization: Catastrophic vs. Parametric Faults

• Catastrophic Faults
  - Catastrophic faults are caused by defects and degrade random yield
  - Random yield is a function of die area
  - Simulation of all catastrophic faults is very computationally intensive

• Parametric Faults
  - Parametric faults are caused by process variation and mismatch
  - Parametric faults cause systematic yield loss
  - Simulation of parametric faults requires process characterization
Which Fault Model is Better (if Any)?

- The Catastrophic Fault Model Enables Creativity in Approaches to Testing
- The Parametric Fault Models Implies a Requirement for Functional Test

- Failure Analysis Results show that Yield Loss is caused by Defects, but…
- Tests designed for Catastrophic Faults have been shown not to Cover All Failures
- Tests for Parametric Faults Cover Catastrophic Faults

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**System Test Issues**

- SOC specs are diverse, making the use of generic solutions difficult
- Some SOC specs are very difficult or expensive to measure
  - Example: RF Tests
- SOCs can contain blocks which are not controllable or observable from I/O pins
- Proposed Approach: Consider the System Architecture and Testability at the Same Time
  - Example: Bluetooth specs may not be measurable through I/Os
  - Testability may require a higher resolution ADC or frequency shifting to enhance signal power
- Alternative: Block-Level BIST

Emerging BIST Solutions for Analog Blocks: Integrated Test Cores

The Tester-on-Chip includes: Arbitrary Waveform Generator and a Waveform Digitizer
• Test signals only need to be propagated short distances, improving signal integrity

Integrated Test Cores

- The Arbitrary Waveform Generator includes a Periodic Bit Stream Generator and an Analog Reconstruction Filter
- The Periodic Waveform Digitizer includes a Programmable Reference and a Comparator
- Advantages
  - Mostly digital implementation, and therefore mostly scalable among technologies
- Issues
  - Implementation requires a significantly higher clock frequency than the frequency of the analog input function
  - Performance of any analog blocks (such as the analog filter) will vary with the manufacturing process (and variations may correlate with the analog block being tested)
A/D Converters

- Two of the key specs for A/D Converters are integral nonlinearity (INL) and differential nonlinearity (DNL).
- INL and DNL are a function of the code transition voltages.
- Computing INL and DNL consume 35-50% of test time.

\[
\text{DNL}(i) = \frac{(x(i)-x(i-1))}{\text{1 LSB}} - 1
\]

\[
\text{INL}(i) = \frac{x(i)-x(1)-(x(2^n-1)-x(1))(i-1)/(2^n-2)}{\text{1 LSB}}
\]

Digital

\(x(i-1)\) \(x(i)\)

Analog

code transition voltages
BIST for A/D Converters

- **Issues**
  - Rise and fall times of the digital signal correlate with the offset measurement
  - If the signal generator contains a lowpass filter, its performance may correlate with measurements
Oscillation-Based BIST for D/A Converters and Filters

• Method
  - Block Under Test is included in a feedback loop which forces oscillation
  - The oscillation frequency is measured with a frequency counter
  - The frequencies are converted to measurements, i.e. measurements of DNL and INL for D/A Converters

M.A. Stegawaski, B. Kaminska, and A. Frisch, “Fast and accurate BIST for D/A and A/D converters: the sigma-delta approach.”
Example: BIST for D/A Converters

- Issues
  - Sample size of the digital frequency measurement impacts accuracy and test time
**BIST for PLLs**

- **Method**
  - PLL input is disconnected from external frequency source and controlled by a phase delay circuit or the charge pump
  - The oscillation frequency is measured with a frequency counter
  - Sensitive paths are not touched
  - Circuitry is digital
  - Limited approaches available to measure jitter

**Example: BIST for PLLs**

- **Issues**
  - Phase delay between the BIST circuit and the PLL
  - Sample size of the digital frequency measurement
Implementation of Block-Level BIST

- Implementation of BIST in a system requires considering area and power consumption overhead and the impact on design schedules
- We need to consider
  - How to partition the system into blocks
  - Sharing BIST circuitry among blocks
  - Impact of routing signals to and from BIST circuit (Can routing be reduced by using redundant BIST blocks?)
  - Minimize the use of analog blocks to maximize chances of first-pass design success

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Summary

- As the semiconductor industry disaggregates, testing will need to become “smarter” to detect manufacturing problems
- New technologies and SOCs have resulted in the emergence of new failure mechanisms, which require new fault models
- Traditional failure and yield analysis techniques are becoming less effective as technology scales
- The rise in the cost of test as a fraction of manufacturing cost is pushing the industry to experiment with BIST and low cost testers
Summary

- Commercial BIST solutions are emerging for digital logic, memory, and mixed-signal circuits, but mixed-signal BIST lags in terms of industrial acceptance.
- Availability of mixed-signal BIST may limit the ability to migrate to low cost testers.
- Several approaches to system-level and block-level BIST have been discussed, including block-level solutions for:
  - A/D Converters
  - D/A Converters
  - Filters
  - PLLs