Curriculum Vitae
Prof. Antonio Núñez

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Short resume

Antonio Nunez was born in Madrid, Spain, in 1951. He received the higher engineering degree in 1974 from the School of Telecommunication Engineering at the Technical University of Madrid UPM, and the Ph. D. degree also from UPM in 1981. From 1974 to 1976 he worked as a Consultant for Telefonica. He was a Research Scientist with the Electrical Engineering Department of EPFL Lausanne, Switzerland, in 1981, working in CMOS processor design, and a Visiting Scientist (1986-1987) and Visiting Professor (1987-1988) at the School of Electrical Engineering of Purdue University, USA, working in compound semiconductor high-speed VLSI design and processor design for critical real time applications. He also spent a shorter summer stay at the Department of Electrical Engineering, Stanford University. He was appointed Titular Professor at the University of Las Palmas GC, in 1982, and Professor in 1989. Among other academic positions he has served as director of the Department of Electronics, director of the Institute for Applied Microelectronics, and dean of the School of Telecommunication Engineering of ULPGC. He has published five books, over 40 journal papers, and over 100 conference papers. He has supervised 11 PhD theses. His current research fields include heterogeneous architecture platform based design and hardware-software co-design for embedded systems, communication architecture synthesis for MPSoC, multimedia processor architectures, DVB, DAB, DMB, MPEG4, AVC and SVC codec design, smart imaging processors, and low power optimization of integrated circuits. He is a member of IEEE Circuits and Systems Society, the European Association for Design Automation, and Euromicro, the European Association for Microelectronics and Computing. He is also in the steering committees of ISQED, Euromicro, DSD, and DCIS. Antonio Núñez has served as General Chairman or Program Committee Chairman of several conferences in the field. He is associate editor of Elsevier Journal of Systems Architecture, Springer Journal of Real Time Image Processing, and Hindawi Journal of Embedded Systems.

Research Stays

(1983): Laboratoire de Systemes Logiques. École Polytechnique Federale de Lausanne (Switzerland), Dèpartement d'Electricité. Profs. Daniel Mange, Eduardo Sanchez (and Murat Kunt): October, November, December 1983. Research on VLSI, Microarchitectures and Microprogramming

(1986-1988): GaAs Digital Systems Design Laboratory, Department of Computer Engineering, School of Electrical Engineering, Purdue University, USA, Prof. D. Meyer, J. Fortes and V. Milutinovic. June 1986-October 1986: previous stay at Stanford, Prof. E.J. McCluskey, research on clock distribution and interconnects in very high speed digital integrated circuits. Purdue: October 1986-January 1988. Stay as Visiting Scientist 86/87 and Visiting Professor 87/88. Research on processor microarchitecture and VLSI design for very high speed technologies in Silicon and GaAs. Development of a DSP-VLIW processor mapped both in Silicon and GaAs technologies. Teaching of course EE696 "Processor Design Projects"

Publications-1
Papers in journals

(last 20 years)

M. Sánchez, J.A. Méndez and A. Núñez,
"The Concentrating/Diffussing System for a Communication Cluster Controller",
Microprocessing and Microprogramming, 16:163-167, 1985

A.Núñez,
"A Survey of GaAs Computer Design",
Microprocessing and Micoprogramming, 21:665-670, 1987

A.Núñez, R.Sarmiento, P.P.Carballo,
"Some Results in GaAs Processor Design using LSI Integrated Circuits",
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A.Núñez, D.Carnal,
"MVM: A GaAs Microprocessor for Critical Real-Time Applications",
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A.Núñez and D.Fay eds,
"Hardware and Software Design Automation",
North-Holland, Elsevier, 1991

L.Ferragut, R.Montenegro, G.Winter, A.Núñez,
"Accurate Extraction of Interconnect Capacitances by Adaptive Mixed Finite Element Method",
Microprocessing and Microprogramming, 32:61-68, 1991

K.Eshraghian, R.Sarmiento, P.P.Carballo, A.Núnez,
"Speed-Area-Power Optimization for DCFL and SDCFL Class of Logic Using Ring Notation",
Microprocessing and Microprogramming, 32:75-82, 1991

B. Graff Mortensen and A. Núñez, eds,
"Hardware and Software, Specification and Design",
North Holland, Elsevier, 1992

P. Milligan and A. Núñez, eds,
"Parallel and Distributed Processing",
IEEE Computer Society, Los Alamitos, California, 1992

L. Gómez, A. Hernández and A. Núñez,
"Timing Model for SDCFL Digital Circuits".
Microprocessing and Microprogramming, 34:193-196, 1992

R. Sarmiento, P.P. Carballo and A. Núñez,
"High Speed Primitives of Hardware Accelerators for DSP in GaAs Technology",
Institute of Electrical Engineers, Proceedings G, Vol. 139, no.2, April, pp.205-216, 1992

A. Hernández, L. Gómez and A. Núñez,
"An Empirical Model to Estimate Power Consumption in GaAs DCFL/SDCFL Circuits",
Microprocessing and Microprogramming, 37: 23-26, 1993

R. Sarmiento, P.P. Carballo and A. Núñez,
"Integer and Control Units of a 32-bit GaAs Processor",
Microprocessing and Microprogramming, 37:105-108, 1993

L. Gómez, A. Hernández, and A. Núñez,
“Timing Analysis for DCFL/SDCFL VLSI Circuits”,
Microprocessing and Microprogramming, 38: 511-518, 1993

L. Gómez, A. Hernández, and A. Núñez,
“Multiobjective Optimization Using Analytical Models of GaAs High-Speed Digital Circuits”,
Microprocessing and Microprogramming, 39: 267-270, 1993

J.F. López, K. Eshraghian, R. Sarmiento and A. Núñez,
“Gallium Arsenide Pseudo-Dynamic Latched Logic”,
IEE Electronics Letters, vol. 32, pp.1353-1354, July, 1996
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J.F. López, R. Sarmiento, K. Eshraghian and A. Núñez,
“Noise Margin Enhancement in GaAs ROMs using Current Mode Logic”,
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J.F. López, K. Eshraghian, R. Sarmiento, A. Núñez and D. Abbott,

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R. Sarmiento, F. Tobajas, V. De Armas, R. Esper-Chain, J.F. López, J. Montiel and A. Núñez,
"A CORDIC Processor for FFT Computation and its Implementation using Gallium Arsenide Technology",
IEEE Transactions on Very Large Scale Integrated Systems, Vol. 6, No. 1, pp.18-31, March, 1998

J.F. López, R. Reina, L. Hernández, F. Tobajas, V. De Armas, R. Sarmiento and A. Núñez,
" GaAs Pipelined Carry Lookahead Adder",
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"Quality factor model for integrated inductors in CMOS technology",
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"Models and Tools for CMOS Integrated Inductors",
Int. Journal of Analog Integrated Circuits and Signal Processing, vol. 33, págs. 171-178, 2002

B.D. Theelen, A.C. Verschueren, V.Reyes, M.P.J. Stevens, A. Núñez,
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Vector Plus, no. 24, pp. 14-23, 2004

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"Characterization of extrinsic resistances in temperature behaviour modelling of InGaAs MODFET´s",
Semiconductor Science and Technology, vol. 19, no. 5, pp. 648-654, 2004

G.M. Callicó, S. López, R.P. Llopis, J.F. López, A. Núñez, R. Sethuraman and R. Sarmiento,
"Low-cost Super-Resolution Algorithms Implementation over a HW/SW Video Compression Platform",
Eurasip Journal on Applied Signal Processing, Special Issue on Super-Resolution, accepted for publication, vol. 2006, pp. 1-31

A. Núñez,
"Advances in video coding for hand-held device implementation in networked electronic media",
Springer Journal of Real-Time Image Processing, (survey) accepted for publication, 2006

V. Reyes, W. Kruijtzer, T. Bautista and A. Núñez,
"A SystemC based System-Level Design Tool for Embedded Multiprocessor Systems Modeling and Simulation",
ACM Transactions on Embedded Computing Systems, accepted for publication, 2006

L. García, V. Reyes, D. Barreto, G.M. Callicó, T. Bautista and A. Núñez,
"Towards a Configurable SoC MPEG-4 Advanced Simple Profile Decoder"
IEE Proc. Computers & Digital Techniques, accepted for publication, 2006

Publications-2
Papers in Conference Proceedings

(last 15 years)

A. Hernández, L. Gómez and A. Núñez,
"Modelo para Análisis Temporal de Circuitos Digitales SDCFL",
Proc. VI Congreso de Diseño de Circuitos Integrados, pp. 425-430, Santander (Spain), 1991

L. Gómez, A. Hernández, and A. Núñez,
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A. Hernández, L. Gómez and A. Núñez,
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"Multiobjective Optimization Using Analytical Models of GaAs High-Speed Digital Circuits,"
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Proceedings of the 3rd International Workshop on Design Automation, pp 226-233, Moscow (Russia), 1993

S. Perdomo and A. Núñez,
"Results of Analyzing VLSI Interconnect Structures by a Methodology Based on Mixed Frequency-Time Domain",
Proc. European Conference on Design Automation with EUROASIC Event, EDAC'93, Paris, France, pp. 409-413, IEEE Computer Society Press, 1993

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Proceedings of the 3rd International Workshop on Design Automation, pp 203-225, Moscow (Russia), 1993

L. Gómez, A. Hernández, and A. Núñez,
"Optimization Using Analytical Models of GaAs High-Speed Digital Circuits",
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A. Hernández, L. Gómez and A. Núñez,
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Proceedings of the European Design Automation Conference, pp 190-195, Hamburg (Germany), 1993

J.A. Montiel, V. Armas, D. Fay and A. Núñez,
"Using ES2 Library and SILOS Simulator in the Development of a Single Chip with Three Processors and Analog I/O",
In: P. Milligan and A. Núñez, eds., Proceedings of the Parallel and Distributed Processing Workshop PDP93, pp. 359-368, IEEE Computer Society, 1993

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"Delay, Power and Area Expressions of GaAs High-Speed DCFL Circuits and their Applications to Optimization",
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J.F. López, K. Eshraghian, A. Núñez and R. Sarmiento,
“Gallium Arsenide MESFET Memory Architectures”,
Proc. IEEE International Workshop on Memory Technology, Design and Testing, San José, California, August 1995

A. Núñez,
"Tradeoffs in VLSI Architecture for High-Performance Signal Processing",
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J.F. López, R. Sarmiento, A. Núñez and K. Eshraghian,
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“High Performance Pseudo-Dynamic Classes of Logic”,
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L. Hernández, F. Tobajas, J.F. López, R. Sarmiento, A. Núñez and K. Eshraghian,
“Current Mode Techniques for Embedded GaAs ROM”,
Proc. Integrated Circuits and Systems Design Conference, DCIS’96, Sitges, Spain, November, 1996

A. Núñez, R. Sarmiento, R. Esper-chaín, J. Jakobsen, J.F. López, J. Montiel, V. De Armas, and F. Tobajas,
"GaAs ICs for 10 GB/s ATM Switching",
Proceedings IEEE GaAs IC Symposium, Anaheim, California, October 12-15, 1997, pp. 101-104, Invited paper

J. del Pino, A. Hernández, B. González, J. García, and A. Núñez,
"Performance Analysis and Propagation Delay Time Estimation of Logic Families with HBTs",
Proceedings of the XII Design of Circuits and Integrated Systems Conference, pp 459-464, Seville (Spain), 1997

J. García, A. Hernández, B. González, J. del Pino, and A. Núñez,
"Timing Analysis Model Based on Sensitivity for DCFL Family with HFET's",
Proceedings of the XII Design of Circuits and Integrated Systems Conference, pp 453-457, Seville (Spain), 1997

B. González, A. Hernández, J. García, and A. Núñez,
"Influence of temperature and doped layer concentration on P-HFETs",
Proceedings of the International Symposium on IC Technology, Systems & Applications, ISIC'97, pp 394-397, Singapore, 1997

J. del Pino, A. Hernández, B. González, J. García, and A. Núñez,
"Performance Analysis and Propagation Delay Time Estimation of Logic Families with HBTs",
Proceedings of the VII International Symposium of Power and Timing Modelling Optimization and Simulation, pp 323-332, Louvain-la-Neuve (Belgium), 1997

L. Hernández, F. Tobajas, J.F. López, R. Esper-Chaín, V. De Armas, R. Sarmiento and A. Núñez,
"A Low Power Pipelined GaAs ROM",
Proceedings DCIS97, Design of Circuits and Integrated Systems Conference, November 18-21, 1997, Seville, Universidad de Sevilla, pp. 435-440

T. Bautista, G. Marrero, P. P. Carballo and A. Núñez,
"Rapid-prototype of High-performance RISC Cores with VHDL,"
Proceedings VIUF Fall 1997 Conference, VHDL International Users' Forum (VIUF), Edited by the IEEE Computer Society, Arlington, Virginia, EE.UU, pp. 43-52, 19-22 October, 1997

R. Sarmiento, C.J. Pulido, V. De Armas, J.F. López, R. Esper-Chaín, J. Montiel and A. Núñez,
"A 600 MHz 2D-DCT Processor for MPEG Applications",
Proceedings of the 31st Asilomar Conference on Signals, Systems and Computers, Monterrey, California, 2-5 November 1997, Invited paper

J. García, A. Hernández, J. del Pino, B. González, and A. Núñez,
"Estimation of Power Consumption Based on Sensitivity Analysis for DCFL with HFET's",

Proceedings of the XIII Design Circuits and Integrated Systems Conference, pp 96-100, Madrid, November, 1998

J. A. Montiel, V. De Armas, R. Sarmiento and A. Núñez,
"A Cell and Macrocell Compiler for GaAs VLSI Full-Custom Design",
Proceedings Design Automation and Test in Europe (DATE), February, 1998, Paris, IEEE Computer Society, pp. 947-948, 1998

A. González, G. Marrero, P.P. Carballo, T. Bautista and A. Núñez,
"Tratamiento de señales en DSPs multiprocesadores. Algoritmo paralelo para MPEG en el sistema SDB TMS320C80",
FAVI, International Conference on Automatic Control. PADI2, Piura, Peru, pp. 71-76, 1-3 October, 1998

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"Application of Sensitivity Analysis in Modelling Power and Delay for HFET DCFL Circuits",
Proceedings PATMOS'98, International Conference on Power and Timing Modeling Optimization and Simulation, October 7-9, Lingby, Denmark, pp. 51-60, Technical University of Denmark, 1998

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T. Bautista and A. Núñez,
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"Design of Efficient SPARC Cores for Embedded Systems",
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T. Bautista and A. Núñez,
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Proceedings of International Symposium on Quality Electronic Design ISQED'2000, San Jose CA USA, March 2000, IEEE Computer Society, pp. 217-226, Best Paper Award

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M. Marrero, P. P. Carballo, G. Marrero and A. Núñez,
"A quantitative approach to analyze and bound the synthesis-to-layout performance-spread of soft IP cores",
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G. M. Callicó, R. Peset-Llopis, A. Núñez, R. Sethuraman, and M. Op de Beeck,
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G. M. Callicó, R. Peset-Llopis, A. Núñez and R. Sethuraman,
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J. Jachalsky, M. Wahle, P. Pirsch, S. Capperon, W. Gehrke, W. Kruijtzer and A. Núñez,
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A. Núñez, V. Reyes y T. Bautista,
"Signalling in the Heterogeneous Architecture Multiprocessor Paradigm",

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"Mapping of Real-Time and Low-Cost Super-Resolution Algorithms on a Hybrid Video Encoder",
Proc. of the SPIE's International Symposium on Microtechnologies for the New Millennium (VLSI Circuits and Systems), SPIE'2003, Maspalomas, Gran Canaria, 2003

M. Marrero, P. P. Carballo and A. Núñez,
"A method of generating trust-worthy performance estimations for soft-IPs",
Proc. of the SPIE's International Symposium on Microtechnologies for the New Millennium (VLSI Circuits and Systems), SPIE'2003, Maspalomas, Gran Canaria, 2003

P. Carballo, M. Marrero and A. Núñez,
"Some experiences using System-on-Chip buses",
Proc. of the SPIE's International Symposium on Microtechnologies for the New Millennium (VLSI Circuits and Systems), SPIE'2003, Maspalomas, Gran Canaria, 2003

B. González, A. Hernández, J. García, J. Pino, J.R. Sendra, and A. Núñez,
"Temperature Extrinsic Modeling in HFETs,"
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"Temperature in HFETs when operating in DC",
Proc. of the SPIE's International Symposium on Microtechnologies for the New Millennium (VLSI Circuits and Systems), SPIE'2003, Maspalomas, Gran Canaria, 2003

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"Empirical model of the metal losses in integrated inductors,"
Proc. of the SPIE's International Symposium on Microtechnologies for the New Millennium (VLSI Circuits and Systems), SPIE'2003, Maspalomas, Gran Canaria, 2003

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"DC -Extrinsic Model for AlGaAs/InGaAs/GaAs HFETs",
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V. Reyes, T. Bautista and A. Núñez,
"A Scalable Communication Platform for High Performance Multimedia Applications",
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"The impact of integrated inductors on low noise amplifiers",
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D. Barreto, L. García, G. M. Callicó, T. Bautista, P. P. Carballo and A. Núñez,
“Super-Resolution over Compresed Video”,
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“ARTEMI: Architectures for Multimedia and Internet”,
Proc. I Jornadas de Microelectrónica Aplicada, Las Palmas de Gran Canaria, July, 2004

C. Ruíz, T. Bautista, G. M. Callicó, P. P. Carballo and A. Núñez,
“Camellia: a Core for Ambient and Mobile intELLigent Imaging Applications”,
Proc. I Jornadas de Microelectrónica Aplicada, Las Palmas de Gran Canaria, July, 2004

V. Reyes, T. Bautista, G. Marrero, P.P. Carballo, W. Kruijtzer and A. Núñez*,
"CASSE: A System-Level Modeling and Design-Space Exploration Tool for Multiprocessor Systems-on-Chip",
Proc. Euromicro Symposium on Digital Systems Design DSD 2004, Architectures, Methods and Tools, Rennes, France, September 2004, pp. 476-483

S. López, G.M. Callicó, J.F. López, R. Sarmiento and A. Núñez,
"A High Quality/Low Computational Cost for Block Matching Motion Estimation",
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G.M. Callicó, S. López, R.P. Llopis, R. Sethuraman, J.F. López, R. Sarmiento and A. Núñez,
"Low Cost Implementation of a Super-Resolution Algorithm for Real-Time Video Applications",
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G.M. Callicó, S. López, R. P. Llopis, R. Sethuraman, A. Núñez, J.F. López, R. Sarmiento and M. Marrero,
"Practical considerations for real-time super-resolution implementation techniques over video coding platforms",
Proc. of the SPIE’s International Symposium on Microtechnologies for the New Millennium (VLSI Circuits and Systems) 2005, Seville, May 2005, vol.5837, pp 613-627

L. García, V. Reyes, D. Barreto, G. M. Callicó and A. Núñez,
"Evaluation of Architectures for an ASP MPEG-4 Decoder using a System-Level Design Methodology”,
Proc. of the SPIE’s International Symposium on Microtechnologies for the New Millennium (VLSI Circuits and Systems) 2005, Seville, May 2005, vol.5837, pp 785-794

D. Barreto, G. M. Callicó, S. López, L. García and A. Núñez,
"Real-Time Super-Resolution over raw and compressed video sequences",
Proc. of the SPIE’s International Symposium on Microtechnologies for the New Millennium (VLSI Circuits and Systems) 2005, Seville, May 2005, vol.5837, pp 628-637

V. Reyes, W. Kruijtzer, T. Bautista, G. Marrero and A. Núñez,
"A Multicast Inter-Task Communication Protocol for Embedded Multiprocessor Systems",
Proceedings of the 3rd IEEE/ACM/IFIP International Conference on Hardware/software Codesign and System Synthesis, CODES + ISSS'05, Jersey City, New Jersey (USA), September 2005, pp 267-272

L. Garcia, V. Reyes, D. Barreto, G. M. Callicó, T. Bautista, A. Núñez,
"Analysis of MPEG-4 Advanced Simple Profile (ASP) Architectures Using a System-Level Design Methodology",
Proc. XX Conference on Design of Circuits and Integrated Systems DCIS'05, Lisbon, Portugal, November 2005, paper 6c.1, 6 pp

V. Reyes, L. García, T. Bautista, G. M. Callicó and A. Núñez,
"Narrowing the Design Productivity Gap: A System-Level Design and Simulation Environment for Heterogeneous MPSoCs",
Proc. IEEE International High Level Design Validation and Test Workshop HLDVT'05, Napa Valley, California, USA, December 2005

V. Reyes, W. Kruijtzer, T. Bautista, G. Alkadi and A. Núñez,
"A Unified System-Level Modeling and Simulation Environment for MPSoC design: MPEG-4 Decoder Case Study",
Proc. Conference on Design Automation and Test in Europe, DATE 2006, Munich, March 6-10, 2006

A. Sanchez-Peña, P.P. Carballo, L. Garcia and A. Núñez,
"VIPACES, Verification Interface Primitives for the development of AXI Compliant Elements and Systems",
Proc. Euromicro Conference on Digital System Design, DSD 2006, Catvat, Croacia, August, 2006

A. Sanchez-Peña, P.P. Carballo, L. Garcia and A. Núñez,
"Analysis of Data Load per Component and Communication Channels using an AMBA 3 AXI Verification Library for SoC",
Proc. XXI Conference on Design of Circuits and Integrated Systems DCIS'06, Barcelona, 2006

L. Garcia, D. Barreto, P.P. Carballo, G. M. Callicó and A. Núñez,
"Design of an MPEG-4 ASP SoC with novel Super-Resolution Enhancements for DAB channels",
Proc. XXI Conference on Design of Circuits and Integrated Systems DCIS'06, Barcelona, 2006

PARTICIPATION IN INTERNATIONAL COMMITTEES

Main activity and services:

Steering Committee, ISQED, member since 2001

ISQED Program Committee, member since 2000

Steering Committee, DSD, member since 1998

DSD Program Committee, member since 1998

EUROMICRO Board of Directors, member, since 1992. EUROMICRO, The European Association for Microelectronics and Computing. Member since 1985

Steering Committee, DCIS, member since 1996

EUROMICRO Program Committee member since 1988

Cofounder and Program Committee member, EUROMICRO Parallel, Distributed and Network-based Processing Conference, PDP, 1993-2000

Program Committee member, SPIE's Symposium on Microtechnologies for the New Millennium: VLSI Circuits and Systems, 2003, 2005 and 2007

Cofounder and Program Committee member, PATMOS (Power and Timing Modeling, Optimization and Simulation), since 1989

Sample of other international services:

Chairman of the Program Committee and co-chair of the inaugural plenary session, IV International Design Automation Workshop, Russian Academy of Science, Moscow, Russia, 1994

Chairman of the Best Paper Award Selection Committee, ISQED 2006, San José, California, USA, 2006

Member of the Program Committee and Organizing Committee of the European Design Automation Conference EDAC 93, Paris, later on renamed as European Design and Test Conference ED&TC, and finally DATE

Chairman of the Program Committee, EUROMICRO'91, Vienna, 1991

Chairman of the Program Committee, Digital System Design Conference, Maastricht, 2000

General Chairman of the Conference, and Program Committee member, IX Congreso de Diseño de Circuitos Integrados, DCIS'94, Gran Canaria, 1994

General Chairman of the IFIP/TC10/WG2 Workshop "CAE Environments for Processor Design and Processor-based Design", Gran Canaria, May, 1992

Program Committee member and Coordinator of the “Architecture” area, EUROMICRO'89, Colon, 1989

Program Committee member and Coordinator of the “Architecture” area, EUROMICRO'88, Zurich, 1988

General Chairman, European Workshop on Parallel & Distributed Processing, Las Palmas GC, January 1993, organized by EUROMICRO and EEC-ESPRIT

Chairman of the Program Committee, European Workshop on Power and Timing Modeling Optimization and Simulation PATMOS'92, Paris, September 1992, organized by EEC-ESPRIT and EUROMICRO

Deputy Program Chairman, EUROMICRO'92, Paris, 1992.

Keynote Address, ESPRIT Conference, Emerging Technologies, Brussels, 1988

Keynote Address, IEE Microelectronics Conference, Adelaide 1995

MISCELANEOUS

Coordination of large international consortia
General Coordinator of MUSICCA “Microelectronics Wireless Systems for Industrial Communication-and-Control Applications”, proposal for a Network of Excellence in Microelectronics Design, for the Sixth Framework Program of Research, European Community, IST Priority, formed by 20 European universities and research centers (ETH, EPFL, KTH, IMEC, CSEM, VTT, INESC, KUL, UCL, U Sheffield, U Sussex, U Roma La Sapienza, Politecnico di Torino, U Bolonia, U Catania, FhG IIS Erlangen, INP, CNRS, CRL, CarinthiaTech) jointly with 5 spanish universities and 15 companies. The proposal was approved by the scientific evaluation committee, but finally it was not funded. June 2003.

Editor
Associate editor:
- Elsevier Journal of Systems Architecture
- Hindawi Journal of Embedded Systems
- Springer Journal of Real Time Image Processing

Comissions
Member of 49 PhD committees, among them 2 at Purdue University (USA), 1 at Eindhoven University of Technology (Holland), 1 at Ecole Nationale Superieure des Telecommunications, ENST (Paris), and 1 at Edith Cowan University, Perth (Australia); as well as 1 Master Thesis committee at The University of Adelaide (Australia).
Evaluator of ~20 projects for the National Plan of Research, Areas ICT and ECT
Member of the National Panel in charge of drafting the National Plan for Research 2000-2003, area ICT (12 members)
Member of the National Commission in charge of evaluating and supervising national projects in area ECT, 2006

Reviewer
Reviewer (over 50 reviews) for the journals:
- IEEE Transactions on Circuits and Systems
- IEEE Transactions on VLSI
- IEEE Journal of Solid State Circuits
- Butterworth Microprocessor Systems
- Elsevier Microprocessing and Microprogramming
- Elsevier Journal of Systems Architecture
- Springer Journal of Real Time Image processing
- Hindawi Journal of Embedded Systems

Reviewer (over 300 reviews) for many conferences including EDAC, ED&TC, DATE, ISQED, EUROMICRO, PDP, DSD, PATMOS, ESSCIRC, VLSI, DDECS, DCIS.

Some overseas research centers visited by invitation:

Laboratoire de Systemes Logiques. Département Electricité. École Polytechnique Fédérale de Lausanne. (Switzerland).
Centre Electronique Horloger de Neuchatel, and CSEM (Switzerland).
Department of Electrical Engineering. Stanford University (USA).
GaAs Digital Systems Design Laboratory. School of Electrical Engineering. Purdue University (USA).
Department of Electrical Engineering. College of Engineering. Notre Dame University (USA).
Department of Electrical Engineering. College of Engineering and Applied Sciences. State University of New York at Stony Brook
INESC, Instituto de Engenharia de Sistemas e Computadores. Lisbon (Portugal).
Electrical Engineering and Computer Science Department. Research Laboratory of Electronics. Massachusetts Institute of Technology
Département Electronique. École Nationale Supérieure des Télécommunications (ENST). Paris (France).
Lehrstuhl für Rechnerorganisation. Fachbereich Informatik. Universität Kaiserslautern. (Germany).
Centre for Microelectronic Systems Applications. School of Electronic System Engineering. The Polytechnic of Central London
Department of Electrical Engineering and Computer Science. University of California Berkeley (USA).
Department of Electrical Engineering and Computer Science. University of California Santa Cruz (USA).
Department of Electrical Engineering. University of Santa Clara (USA).
Fachbereich Informatik. ETH Zürich (Switzerland).
Dipartamento di Elettronica. Politecnico di Milano (Italy).
Department of Electronics Digital Systems Design Laboratory. Eindhoven University of Technology (Holland).
NIISAPRAN (CAD for VLSI Research Centre), Russian Academy of Sciences, Moscow, Russia.
Centre for GaAs VLSI Technology, The University of Adelaide (Australia).
Department of Computer Engineering and Communications, Edith Cowan University, Perth (Australia).
Facultad de Ingeniería. Universidad de Piura (Peru).
Facultad de Ingeniería. Escuela Politécnica Nacional de Ecuador (Ecuador).