Hitachi’s SuperH™ RISC Family

The SH7751 (SH-4 with PCI) Microprocessor

Hitachi Semiconductor (America) Inc.
San Jose, CA
SuperH Core Roadmap

SH-1
12-20 MHz
4 Designs

SH-2
16-40 MHz
14 Designs

SH-2E
40 MHz
2 Designs

SH-2 DSP
60-66 MHz
2 Designs

SH-3
45-133 MHz
6 Designs

SH-3E
100 MHz
1 Design

SH-3 DSP
133 MHz
1 Design

SH-4
128-200MHz
3 Designs

SH-5

80 Million Units Shipped
Newest SH-4: SH7751

Features

- Integrated PCI version 2.1
- Performance/Power optimized
  1,000 MIPS / Watt @ 133 MHz
- Two versions:
  133 MHz (240 mW) @ 1.5 V
  167 MHz (400 mW) @ 1.8 V
- 2 way superscalar CPU with
  FP Arithmetic Accelerator:
  300 MIPS, 1.2 GFLOPS @ 167MHz
- Advanced on-chip debug
- 0.18-micron Technology
  55 mm²
  256-pin QFP
Power Optimized Design

1) Reduced activation of cache [13% Reduction]
2) Lowered clock load by reduced W in flipflops [16%]
   → No performance loss due to reduced internal IR
3) Reduced W in datapath cells [9%]
   → No performance loss due to very short interconnect
4) Debug logic not clocked unless used [6%]
5) Process shrink [8%]
6) Standby Vbb control [85%]

<table>
<thead>
<tr>
<th>Improvement</th>
<th>Active</th>
<th>Standby</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>42%</td>
<td>85%</td>
</tr>
</tbody>
</table>
Low Power SuperH Roadmap

- SH-3 SH7708 (200 MIPS/W (60 MHz))
- SH-3 DSP SH7729 (690 MIPS/W (133 MHz))
- SH-4 SH7750 (575 MIPS/W (128 MHz))
- 0 MIPS/W
- 1,000 MIPS/W
- '97
- '98
- '99
Low Power SuperH Roadmap

- **SH-3 SH7708**
  - 200 MIPS/W (60 MHz)

- **SH-3 DSP SH7729**
  - 690 MIPS/W (133 MHz)

- **SH-4 SH7750**
  - 575 MIPS/W (128 MHz)

- **SH-4 PCI SH7751**
  - 1,000 MIPS/W (133 MHz)

- 1,000 MIPS/W

Years:
- '97
- '98
- '99
Low Power SuperH Roadmap

MIPS/W

2,000

1,000

200 MIPS/W (60 MHz)

SH-3 SH7708

'97

SH-3 DSP SH7729

690 MIPS/W (133 MHz)

SH-4 SH7750

575 MIPS/W (128 MHz)

'98

SH-4 PCI SH7751

1,000 MIPS/W (133 MHz)

2,000 MIPS/W

'99

Future SH-4

Future

Hitachi Semiconductor (America) Inc.
SH7750 Key Features

- **CPU**: 2-way Superscalar 128MHz (1.5V), 167/200 MHz(1.8V), 100MHz bus
- **Cache**: Direct Mapping
- **FPU**: Supports IEEE 754 compliant data type
- **MMU**: 4 Gbytes address space
- **DMAC**: Single and dual address modes
- **BSC**: Glueless interface to SDRAM, DRAM, EDO and burst ROM, 7 chip selects
- **INTC**: 5 external interrupt pins
- **WDT**: Watch Dog Timer
- **CPG**: Programmable clock for CPU, bus & peripherals
- **Debug**: JTAG
- **User Break Control (H/W breakpoints)**
- **Timer**: 3 x 32-bit, auto reload
- **RTC**: Supports calendar function
- **SCI**: 1 x 16-bit, full duplex, async/sync
- **SCIF**: 1 x 16-bit with FIFO, full duplex, async
- **I/O**: 20-pins
- **Package**: 208-pin LQFP, 256-pin BGA
## SH7751 Key Features

<table>
<thead>
<tr>
<th>Feature</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>CPU</strong></td>
<td>2-way Superscalar 128MHz (1.5V), 167 (1.8V), 87MHz bus</td>
</tr>
<tr>
<td><strong>Cache</strong></td>
<td>Direct Mapping</td>
</tr>
<tr>
<td><strong>FPU</strong></td>
<td>Supports IEEE 754 compliant data type single and double precision</td>
</tr>
<tr>
<td><strong>PCI</strong></td>
<td>33/66 MHz, 32-bit bus Rev 2.1</td>
</tr>
<tr>
<td><strong>MMU</strong></td>
<td>Supports 4 Gbytes address space</td>
</tr>
<tr>
<td><strong>DMAC</strong></td>
<td>Single and dual address modes</td>
</tr>
<tr>
<td><strong>BSC</strong></td>
<td>Glueless interface to SDRAM, DRAM, EDO and burst ROM. 7 chip selects</td>
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<tr>
<td><strong>INTC</strong></td>
<td>5 external interrupt pins</td>
</tr>
<tr>
<td><strong>WDT</strong></td>
<td>Watch Dog Timer</td>
</tr>
<tr>
<td><strong>CPG</strong></td>
<td>Programmable clock for CPU, external bus &amp; peripherals</td>
</tr>
<tr>
<td><strong>Debug</strong></td>
<td>JTAG</td>
</tr>
<tr>
<td><strong>User Break Control</strong></td>
<td>(H/W breakpoints)</td>
</tr>
<tr>
<td><strong>Realtime/full instruction trace</strong></td>
<td></td>
</tr>
<tr>
<td><strong>Timer</strong></td>
<td>3 x 32-bit, auto reload</td>
</tr>
<tr>
<td><strong>RTC</strong></td>
<td>Supports calendar function</td>
</tr>
<tr>
<td><strong>SCI</strong></td>
<td>1 x 16-bit, full duplex, async/sync</td>
</tr>
<tr>
<td><strong>SCIF</strong></td>
<td>1 x 16-bit with FIFO, full duplex, async</td>
</tr>
<tr>
<td><strong>I/O</strong></td>
<td>20-pins</td>
</tr>
<tr>
<td><strong>Package</strong></td>
<td>256-pin QFP</td>
</tr>
</tbody>
</table>

- **SH-4** 167MHz
- **DMA Controller** 4 channel
- **Bus State Controller**
- **INTC**
- **WDT**
- **CPG / PLL**
- **Debug**
- **I/O**
- **Cache** 8KB Instruction 16KB Data
- **FPU**
- **PCI Bus Controller**
- **RTC**
- **SCI 1 channel**
- **SCIF 1 channel**
# SH7750 and SH7751

<table>
<thead>
<tr>
<th></th>
<th>SH7750 (64 bit SH bus)</th>
<th>SH7751 (32-bit SH/PCI)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency (CPU)</td>
<td>128 MHz</td>
<td>133 MHz</td>
</tr>
<tr>
<td></td>
<td>167 MHz</td>
<td>167 MHz</td>
</tr>
<tr>
<td></td>
<td>200 MHz</td>
<td></td>
</tr>
<tr>
<td>Frequency (Bus)</td>
<td>64 MHz</td>
<td>66.5 MHz</td>
</tr>
<tr>
<td></td>
<td>83.5 MHz</td>
<td>83.5 MHz</td>
</tr>
<tr>
<td></td>
<td>100 MHz</td>
<td></td>
</tr>
<tr>
<td>Vcc (core)</td>
<td>1.5V</td>
<td>1.5V</td>
</tr>
<tr>
<td></td>
<td>1.8V</td>
<td>1.8V</td>
</tr>
<tr>
<td></td>
<td>1.8V</td>
<td></td>
</tr>
<tr>
<td>Vcc (I/O)</td>
<td>3.3V</td>
<td>3.3V</td>
</tr>
<tr>
<td></td>
<td>3.3V</td>
<td>3.3V</td>
</tr>
<tr>
<td></td>
<td>3.3V</td>
<td></td>
</tr>
<tr>
<td>MIPS</td>
<td>230</td>
<td>240</td>
</tr>
<tr>
<td></td>
<td>300</td>
<td>300</td>
</tr>
<tr>
<td></td>
<td>360</td>
<td></td>
</tr>
<tr>
<td>Power (normal/sleep)</td>
<td>400mW 75mW</td>
<td>240mW 50mW</td>
</tr>
<tr>
<td></td>
<td>700mW 120mW</td>
<td>400mW 100mW</td>
</tr>
<tr>
<td></td>
<td>900mW 150mW</td>
<td></td>
</tr>
<tr>
<td>Package</td>
<td>208-LQFP</td>
<td>256-QFP</td>
</tr>
<tr>
<td></td>
<td>208-LQFP</td>
<td>256-QFP</td>
</tr>
<tr>
<td></td>
<td>256-BGA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>256-QFP</td>
<td></td>
</tr>
</tbody>
</table>
SH-4 Registers

General Register
- R0
- R1
- R2
- R7
- R14
- R15

Control Registers
- SR: Status Register
- MACH: Multiply and Accumulator HIGH
- MACL: Multiply and Accumulator LOW
- PR: Procedure Register
- GBR: Global Base Register

System Registers
- MD, RB, BL, FD, M, Q, IMASK, S, T

Program Counter
- PC: Program Counter

Kernel Bank Register
- R0
- R1
- R2
- R7

System Bank Register
- R0
- R1
- R2
- R7

SSR: Saved Status Register
SGR: Saved General Register
VBR: Vector Base Register
DBR: Debug Vector Base Register

SPC: Saved Program Counter

: added at Privileged mode
Two-way Superscalar

Execute Two Instructions in Parallel

Diagram showing the flow of instructions through the superscalar architecture, including the Instruction queue, Decoder1, Decoder2, Branch unit (BR), Integer unit (EX)(MT), Load/store unit (LS)(MT), and Floating point unit (FE).
# Five Stage Pipeline

<table>
<thead>
<tr>
<th>Integer Unit Pipeline</th>
<th>Instruction Fetch</th>
<th>Decode</th>
<th>Execute</th>
<th>Memory Access</th>
<th>Store</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>FPU Pipeline</th>
<th>Instruction Fetch</th>
<th>Decode</th>
<th>Execute</th>
<th>Memory Access</th>
<th>Store</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>Load / store Unit Pipeline</th>
<th>Instruction Fetch</th>
<th>Decode</th>
<th>Execute</th>
<th>Memory Access</th>
<th>Store</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>Branch Unit Pipeline</th>
<th>Instruction Fetch</th>
<th>Decode</th>
<th>Execute</th>
<th>Memory Access</th>
<th>Store</th>
</tr>
</thead>
</table>
FP Arithmetic Accelerator

Two 128-bit simultaneous data transfers
Four fmuls in one cycle
4-input fadd in one cycle
SH-4 for 3D Game Reality in Dreamcast™

“The SH-4’s superscalar execution, fast FP, and high-speed memory bus allow Dreamcast to deliver unprecedented 3D graphics gaming experience to consumers.”

Hideki Sato
Corporate Senior Vice President
Consumer Products Business Group
SEGA Enterprises, LTD. March 1999
Versatility of the SH-4 Arithmetic Accelerator

A single SH-4 instruction, FTRV, can perform this matrix-vector multiplication every 4 cycles.
Versatility of the SH-4 Arithmetic Accelerator

3D Graphics Geometry (1.2 GFLOPS)

\[
\begin{pmatrix}
Y_1 \\
Y_2 \\
Y_3 \\
1
\end{pmatrix} =
\begin{pmatrix}
c_{11} & c_{12} & c_{13} & c_{14} \\
c_{21} & c_{22} & c_{23} & c_{24} \\
c_{31} & c_{32} & c_{33} & c_{34} \\
c_{41} & c_{42} & c_{43} & c_{44}
\end{pmatrix} \times
\begin{pmatrix}
x_1 \\
x_2 \\
x_3 \\
1
\end{pmatrix}
\]

A single SH-4 instruction, FTRV, can perform this matrix-vector multiplication every 4 cycles.

16-tap, 40-sample Block FIR (1.6 MACs/cycle)

\[
\begin{pmatrix}
Y_i \\
Y_{i+1} \\
Y_{i+2} \\
Y_{i+3}
\end{pmatrix} =
\begin{pmatrix}
x_i \\
x_{i-1} \\
x_{i+1} \\
x_i \\
x_{i+2} \\
x_{i+1} \\
x_i \\
x_{i+3} \\
x_{i+2} \\
x_{i+1} \\
x_i
\end{pmatrix} \times
\begin{pmatrix}
c_0 \\
c_1 \\
c_2 \\
c_3
\end{pmatrix} + \ldots +
\begin{pmatrix}
x_{i-12} \\
x_{i-13} \\
x_{i-14} \\
x_{i-15}
\end{pmatrix} \times
\begin{pmatrix}
c_{12} \\
c_{13} \\
c_{14} \\
c_{15}
\end{pmatrix}
Versatility of the SH-4 Arithmetic Accelerator

3D Graphics Geometry (1.2 GFLOPS)

\[
\begin{bmatrix}
Y_1 \\
Y_2 \\
Y_3 \\
1
\end{bmatrix} = \begin{bmatrix}
c11 & c12 & c13 & c14 \\
c21 & c22 & c23 & c24 \\
c31 & c32 & c33 & c34 \\
c41 & c42 & c43 & c44
\end{bmatrix} \times \begin{bmatrix}
x_1 \\
x_2 \\
x_3 \\
1
\end{bmatrix}
\]

A single SH-4 instruction, FTRV, can perform this matrix-vector multiplication every 4 cycles.

16-tap, 40-sample Block FIR (1.6 MACs/cycle)

\[
\begin{bmatrix}
Y_i \\
Y_{i+1} \\
Y_{i+2} \\
Y_{i+3}
\end{bmatrix} = \begin{bmatrix}
x_i & x_{i-1} & x_{i-2} & x_{i-3} \\
x_{i+1} & x_i & x_{i-1} & x_{i-2} \\
x_{i+2} & x_{i+1} & x_i & x_{i-1} \\
x_{i+3} & x_{i+2} & x_{i+1} & x_i
\end{bmatrix} \times \begin{bmatrix}
c0 \\
c1 \\
c2 \\
c3
\end{bmatrix} + \ldots + \begin{bmatrix}
x_{i-12} & x_{i-13} & x_{i-14} & x_{i-15} \\
x_{i-11} & x_{i-12} & x_{i-13} & x_{i-14} \\
x_{i-10} & x_{i-11} & x_{i-12} & x_{i-13} \\
x_{i-9} & x_{i-10} & x_{i-11} & x_{i-12}
\end{bmatrix} \times \begin{bmatrix}
c12 \\
c13 \\
c14 \\
c15
\end{bmatrix}
\]

1024-point, radix-2 FFT (35.4k cycles)

A single DIF butterfly

\[
\begin{bmatrix}
1 & 0 & 1 & 0 \\
0 & 1 & 0 & 1 \\
a & -b & -a & b \\
b & a & -b & -a
\end{bmatrix} \times \begin{bmatrix}
\text{In1}_r \\
\text{In1}_i \\
\text{In2}_r \\
\text{In2}_i
\end{bmatrix} = \begin{bmatrix}
\text{Out1}_r \\
\text{Out1}_i \\
\text{Out2}_r \\
\text{Out2}_i
\end{bmatrix}
\]
PCI Bus Controller

- 32-bit PCI bus controller (Rev 2.1 Compliant)
  - 33 MHz, supports up to 4 device
  - 66 MHz, supports only one device

- Supports Initiator / Target Mode

- PCI Host Arbiter
  - Between PCI devices
  - Between PCI bus and SH4 bus

- PCI operation clock
  - Internal clock
  - external input

- Supports 3.3 V PCI
PCI Bus Controller Con’t

- 4 channel DMA controller
  - 16 deep:32-bit wide FIFO/channel (64 byte)

- Additional 2 FIFOs for target read and write
  - 16 deep:32-bit wide FIFO/channel (64 byte)

- PIO Transfers

- DMA Transfers

- Target Transfers

- PCI bus performance:
  - 132 Mbytes per second @ 33MHz
  - 264 Mbytes per second @ 66MHz
SH7751 PCI Operations

CPU, FPU

Cache, MMU

Mem I/F

Mem I/F

PCI DMAC

PCI I/F

PCI bus

SH bus
PCI PIO Transfer

- CPU direct access of PCI bus memory or I/O via P4 virtual address, bypasses PCI DMAC
  - Memory read and write
  - I/O read and write
  - Supports locked transactions

- Memory access
  - 16Mbyte P4 address allocated for PCI memory access

- I/O Access
  - 256kbyte P4 address allocated for PCI I/O access
SH7751 PIO Transfer
CPU access to PCI

Diagram showing the connection between CPU, FPU, Cache, MMU, Mem I/F, PCI DMAC, PCI I/F, PCI bus, SH bus.
PCI DMA Transfer

- DMA Transfers between PCI device and SH bus
- Memory read and write
- I/O read and write
- Locked transactions not supported
SH7751 DMA Transfer

DMA transfer between SH bus and PCI bus
PCI Target Transfer

- Device on PCI bus direct access SH bus
- Memory read and write
- I/O read and write for accessing PCI local registers
- Supports locked transactions
SH7751 Target Transfer
Target access to SH bus from PCI
Debug Support

- JTAG
  - Downloads
  - Read/write registers and memory
  - Setting breakpoints

- Advanced User Debugger (AUD)
  - Execution trace
## Networking Applications in SH7751

<table>
<thead>
<tr>
<th>Application</th>
<th>Encoder occupancy</th>
<th>Decoder occupancy</th>
<th>Performance</th>
</tr>
</thead>
<tbody>
<tr>
<td>H.263 video (video conferencing)</td>
<td>7% per frame</td>
<td>2.5% per frame</td>
<td>7 - 10 fps; CIF, 128 kbps</td>
</tr>
<tr>
<td>G.723.1 (speech for video conferencing)</td>
<td>16.7% per channel</td>
<td>15% per channel</td>
<td>15 fps; CIF, 128 kbps</td>
</tr>
<tr>
<td>G.729.C (Voice-over-IP)</td>
<td></td>
<td></td>
<td>6 channels 6.3 kbps</td>
</tr>
<tr>
<td>V.90 (software modem)</td>
<td></td>
<td></td>
<td>6 channels 8 kbps</td>
</tr>
</tbody>
</table>

- 6 channels 56 kbps (estimated)
Network System Application
(Single-board 24-channel Modem Pool w/ VoIP server)
Next Generation: Windows CE AutoPC Reference Platform

PCI Bus (33 MHz / 32-bit)

- IEEE-1394 3-Port
- Display
- Graphics/Memory
- MPEG2 decoder

Local Bus (83 MHz / 32-bit)

- Ethernet I/F
- IDE - PCI Bridge - 2 port
- USB 2-Port Host

PCI Bus (33 MHz / 32bit)

- PC card Socket 1
- FLASH 32 MBytes 150 ns
- SDRAM 64 MBytes 83 MHz

Super-I/O Chip Set

- SH-4 w/ PCI
- SH7751

Faceplate
- Audio DSP
- A/D
- CODEC
- GPS receiver
- Microphone
- Radio tuner
- Speaker

IrDA

SRAM
Next Generation: Windows CE Handheld PC-Pro Platform

SH-4 w/PCI SH7751

Graphics Video Audio

Power Supply

ROM 512 Kb

Decoder

FLASH 16 MB

SDRAM 32 MB

Super-I/O Chip

IrDA 1.1

UART

Printer Port

Keyboard

USB

CODEC

AFE

PC Card 1

PC Card 0

LCD/ CRT

NTSC/PAL

AC97

Ethernet
**SH7751 Summary**

- **Connectivity**: On-chip PCI
- **Real Time Debug**: JTAG+AUD Execution trace
- **High Performance Low power**: 1,000 MIPS / W
- **Multimedia**: FP Arithmetic Accelerator (1.2 GFLOPS)

**SH7751 Solution**
SH7751 vs Toshiba TMPR3927F

- SH4, 167MHz (133MHz)
  - Floating Point Unit
  - 8Kbyte instruction cache
  - 16Kbyte data cache
  - 1.8V core (1.5V), 3.3V I/O
  - 256-pin QFP

- PCI - Revision 2.1
  - 32-bit, 4 ch @33MHz
    1 ch @66MHz
  - 3.3V
  - Host, initiator, target
  - Arbiter supports up to 4 PCI devices
  - Dedicated 4 channel DMA with FIFO
  - Target read/write FIFO

- MIPS R3000A, 133MHz
  - 8Kbyte instruction cache
  - 4Kbyte data cache
  - 2.5V core, 3.3V I/O
  - 240-pin QFP

- PCI - Revision 2.1
  - 32-bit, 4 ch @ 33MHz
  - 3.3V
  - Host, initiator, target
  - Arbiter supports up to 4 PCI devices
SH7751 vs AMD Elan SC520

- SH4, 167MHz (133MHz)
  - Floating Point Unit
  - 8Kbyte instruction cache
  - 16Kbyte data cache
  - 1.8V core (1.5V), 3.3V I/O
  - 256-pin QFP
- PCI - Revision 2.1
  - 32-bit, 4 ch @33MHz
  - 1 ch @66MHz
  - 3.3V
  - Host, initiator, target
  - Arbiter supports up to 4 PCI devices
  - Dedicated 4 channel DMA with FIFO
  - Target read/write FIFO

- Am5x86, 133MHz
  - Floating Point Unit
  - 16Kbyte unified cache
  - 2.5V core, 3.3V I/O
  - 388-pin PBGA
- PCI - Revision 2.2
  - 32-bit, 4 ch @ 33MHz
  - 3.3V
  - Host, initiator, target
  - Arbiter supports up to 5 PCI devices
  - FIFO
- Power - ~1.5W
SH7751 vs QED RM5720

- SH4, 167MHz (133MHz)
  - Floating Point Unit
  - 8Kbyte instruction cache
  - 16Kbyte data cache
  - 1.8V core (1.5V), 3.3V I/O
  - 256-pin QFP

- PCI - Revision 2.1
  - 32-bit, 4 ch @33MHz
    - 1 ch @66MHz
  - 3.3V
  - Host, initiator, target
  - Arbiter supports up to 4 PCI devices
  - Dedicated 4 channel DMA with FIFO
  - Target read/write FIFO

- MIPS IV 64-bit RISC
  - Floating Point Unit
  - 32Kbyte instruction cache
  - 32Kbyte data cache
  - 1.8V core, 3.3V I/O
  - 352-pin BGA

- PCI - Revision 2.1
  - 2 x 32-bit , up to 66MHz
  - host bridge function
  - 3.3V
  - Host, initiator, target
  - FIFO

- Power - ~1.5W