Design of SiGe Doherty power amplifier for 5G communications

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Abstract— A Doherty Power Amplifier (DPA) for 5th Generation (5G) wireless applications is presented in this paper. The power amplifier is integrated in IHP 0.13 µm SiGe process. To reduce the area, the Doherty $\lambda/4$ T-Lines are replaced with lumped-elements and custom made solenoid coils are used instead of conventional spiral inductors. The DPA presents a P_{sat} of 23 dBm, a peak PAE of 17.6% and a 13.4 dB gain at 27 GHz. At 9.5 dB output back-off (OBO), it exhibits a 16.9% PAE. The occupied area of the DPA is 1.436 mm x 0.732 mm, including pads.

Index Terms – Doherty PA, Power Added Efficiency (PAE), Output power Back-off (OBO), SiGe, 5G

I. INTRODUCTION

Modern wireless communications such as 5th Generation (5G) are coming with many challenges. Due to presence of large number of independently modulated subcarriers in an Orthogonal Frequency-Division Multiplexing (OFDM) system, the peak power value of the system can be very high as compared to the average power of the whole system. In order to provide high data rates, 5G technology is characterized for having a very high Peak-to-Average Power Ratio (PAPR). As a result, the efficiency at Output Power Back-off (OBO) of the power amplifiers (PA) needs to be improved as well as maintaining high linearity.

For many years, several PA architectures have been reported to solve this challenge by using two back-off efficiency enhancement techniques: bias modulation and load modulation. The Doherty Power Amplifier (DPA) is the most popular solution of load modulation technique [1]. To meet the specifications of high efficiency and linearity, the PA was designed using the IHP 0.13 μ m SiGe process with Heterojunction Bipolar Transistors (HBT). The DPA is described in Section II and simulation results are shown in Section III. In Section IV a comparison is made with several PAs found in the state of the art. Finally, some conclusions are shown in Section V.

II. DOHERTY PA

The block diagram of the DPA is shown in Figure 1, which is composed of a power splitter, a Main (or Carrier) amplifier and an Auxiliary (or Peaking) amplifier. As seen in Figure 1, the Main PA is followed by a $\lambda/4$ transmission line (T-Line), which is added for the proper load modulation. To match the Institute for Applied Microelectronics (IUMA) University of Las Palmas de Gran Canaria Las Palmas de Gran Canaria, España <u>sunil.lalchand@ulpgc.es</u>

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delay through this line, another $\lambda/4$ T-Line is inserted in the input of the Auxiliary amplifier.



Figure 1. DPA block diagram.

The DPA behavior is divided into two operating regions: the low-power region and the back-off region. In the low-power region, only the main PA (Class-B or AB) is turned on, while the auxiliary PA is off due to its Class-C polarization, which needs a higher input signal to produce a current flow. When the main amplifier reaches its saturation and it achieves the first efficiency peak, the Auxiliary amplifier is turned on, entering the back-off region. At maximum output power, the second efficiency peak is achieved. However, the back-off that can be achieved with a conventional Doherty is around 6 dB, and for the new 5G generation it is convenient to have a greater backoff [2]. The back-off can be increased up to 9.5 dB by designing an asymmetric Doherty amplifier, making the main and auxiliary amplifiers of different dimensions. The operation of a conventional Doherty (symmetric) and an asymmetric Doherty is shown in Figure 2.



Figure 2. Symmetric Doherty vs asymmetric Doherty.

A. Design of the DPA

The main amplifier was biased in Class-AB and the auxiliary was polarized in Class-C. The schematic of the DPA is shown in Figure 3, where an asymmetric configuration was adopted. To avoid instabilities, an RC network was added in the main amplifier (R_stab and C_stab) [3]. An asymmetric

Wilkinson power divider was used to provide input/output matching and high isolation between its different ports.

At 27 GHz, the transmission lines take a large area and, as a result, they cannot be integrated into a chip. For this reason, the Wilkinson and the $\lambda/4$ T-lines were designed with lumped elements (π -network). In order to reduce the circuit area, the number of components was reduced by making combinations between the LC networks. The schematic of the DPA is shown in Figure 3.



Figure 3. DPA schematic.

B. Layout implementation of the DPA

To reduce the area that the coils occupy in the circuit, solenoid coils have been designed. These inductors occupy less area than the coils of the technology offered by the IHP Design Kit at the cost of worse quality factors. One of the designed coils can be seen in Figure 4.



The DPA was fully integrated in the SG13S IHP process.

The occupied area is 1.436 mm x 0.732 mm. As seen in Figure 5, RF pads were placed on the left and right edge of the chip and bias pads on the top and bottom.



Figure 5. Layout implementation of the DPA.

III. RESULTS

The PAE, saturated output power and small signal post layout simulation results are shown in Figure 6. The S11 and S22 in the DPA is -20 dB and -34.5 dB respectively, with a small signal gain of 13.4 dB. Regarding output power, 23 dBm value is obtained in the second efficiency peak and the PAE remains above 15% in the back-off region, having a maximum efficiency peak of 17.6%. The back-off obtained is 9.5 dB.



IV. COMPARATIVE

A comparison of our design with state-of-art Doherty PAs is presented in Table I. For the same frequency band, only one Doherty was found in SiGe, so it is compared with amplifiers that, in theory, have better performance because they use a Gallium Arsenide (GaAs) technology. As can be seen, the output power is close to being competitive with GaAs amplifiers. The designed amplifier can be a cheaper alternative than the other circuits reported since the area of our circuit is smaller than the rest of the references and the technology used is cheaper. In addition, the power consumption is much lower considering that it is powered with a lower voltage.

 TABLE I.
 COMPARISON OF PERFORMANCE WITH THE STATE OF THE ART.

Ref.	This work	[4]	[5]	[6]
Tech.	0.13 μm SiGe	0.15 μm GaAs	0.15 μm GaAs	0.13 μm SiGe
Freq (GHz)	27	26.4	25.8	29
DC supply (V)	3.3	5	5	1.7
Psat (dBm)	23	25.3	25.1	19.2
Gain (dB)	13.4	10.3	7	3.8
PAE 6 dB (%)	16	27	12.6	20
Size (mm ²)	1.05	25	2.25	1.87

V. CONCLUSIONS

This paper describes the design and layout implementation of a compact Doherty power amplifier using IHP 0.13 μ m SiGe process (SG13S) for 5G wireless applications. The DPA of this work presents a very compact layout compared to the amplifiers found in the state of the art.

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