Zynq FPGA SoC-based Data Adquisition System for Applications in the Field of Astrophysics

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***Abstract*— This paper describes the design of a FPGA SoC that, integrated in a DAS module, provides a sixteen-channel simultaneous DAS that amplifies at different gains, captures at high speed (256 KSPS) and 24 bit resolution, adds Unix real-time stamps with second or millisecond resolution to the samples, averages the samples and sends the processed signals as binary files to a remote station via Ethernet. This FPGA-based DAS is controlled and configured via commands and an interactive configuration menu. In addition, it shuts down in a controlled manner in the event of a power failure.**

Keywords - DAS; Zynq, ADC; HLS, Zedboard; baremetal application, Validation.

I. INTRODUCTION

The Instituto de Astrofísica de Canarias (IAC), in view of the progress of the QUIJOTE project [1], sees the need to increase the number of polarimeters (up to 60 pixels) and, consequently, to obtain a Data Acquisition System (DAS) capable of amplifying, capturing, and processing their outputs (up to 240 signals) with high sampling rate and resolution (up to 208 KSPS and at least 24 bits) at reasonable costs.

Therefore, the IAC proposes the study, design and development of a scalable unit capable of amplifying, capturing, and processing up to 60 weak analog signals (15 pixels) with 19" and 3U dimensions and a 230 Vac power supply. In addition, they suggest that each module be capable of processing up to 16 weak analog signals (4 pixels) and to synchronize with the rest of the modules to process multiple pixels simultaneously (Fig. 1). The initial specifications of the module are as follows: (1) discrete signal amplification by factors 2 (6dB), 4 (12dB), 6 (16dB), 8 (18dB) and 10 (20dB), allowing selection of these factors via software; (2) analog to digital sample conversion at high sampling rate (up to 208kSP/s) and resolution (at least 24 bits); (3) integration of real-time timestamps to the samples; (4) remote sample storage via Ethernet. All this implemented through an FPGA system that allows reconfiguration of the final system functionality.

II. 16/32 CHANNEL SIMULTANEOUS 24 BITS FAST A/C CONVERTER MODULE

This DAS module has been designed to process up to 32 signals (8 pixels) and, due to its dimensions and the required processing performance, it is composed of electronic components with moderate power consumption. The main subsystems are the following (Fig. 2):

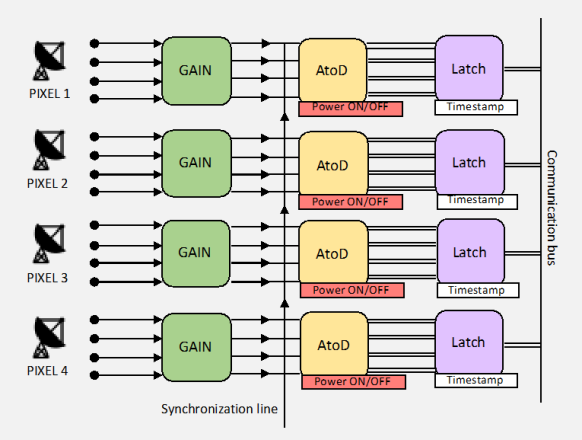

Figure 1. Global scenario for the DAS System

a. A power supply, which supplies the voltages required by the different components of the DAS module from an external voltage of 230 Vac. It has the characteristics of an Uninterruptible Power Supply (UPS). It generates five different power supply voltages (7.3V, 5.4V and 9.7V). In case of external power failure, it has an autonomy of 3.5 minutes and generates a warning signal (AC fail).

b. Two boards composed of sixteen instrumentation amplifiers and two eight-channel AD7768 analogue-to-digital converters from Analog Devices [2], called AD7768 AMP DIFF 16 CH. Each board allows amplification by the factors 1 (0dB), 50 (34dB), 100 (40dB), 200 (46dB) and 300 (50dB) and analog-to-digital conversion of up to sixteen input signals. The choice of these factors is due to the fact that the signals to be received from the Back-End Module (BEM) are of the order of millivolts. The converters feature a maximum sampling rate of 256 KSPS, 24 bit resolution, low current consumption, use sigma-delta conversion techniques and differential inputs. In addition, they are capable of synchronizing with each other in order to digitize more than eight input signals simultaneously and are configurable by pins present on the device or through the SPI protocol.

c. Two FPGA SoC-based ZedBoard from Avnet using the Xilinx SoC Zynq XC7Z020-1CLG484C device [3]. Both

ZedBoard are integrated into the DAS module so that they can control the internal voltage supply, receive the sixteen conditioned signals (amplified and digitized), select the amplification gains and set up the converters through a FPGA Mezzanine Card (FMC) connector and present the processed data on the Ethernet output. The selection of these ZedBoards is because they allow the design of a high performance and low power consumption FPGA System-on-Chip at low cost. They have two ARM Cortex-A9 cores capable of operating at a frequency of up to 866 MHz, it is possible to use one or both of these processors to support symmetric (SMP) or asymmetric (AMP) multiprocessing and its programmable logic (Programmable Logic or PL) includes logic resources such as Look-Up Table (LUT) used for the creation of logic functions, registers and block-type local memory (BRAM), as well as multifunctional DSP blocks for the implementation of multiplication and accumulation operations.

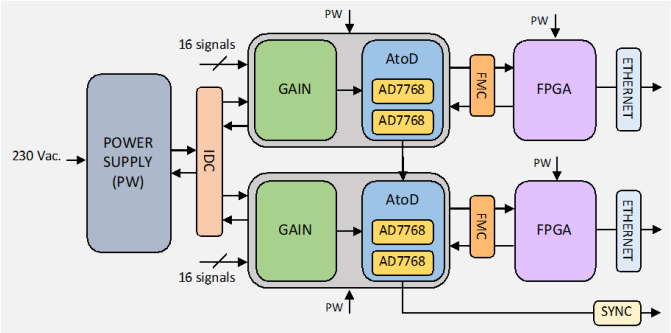

Figure 2. Architecture of the DAS system

III. ARCHITECTURE DESIGN

To design the digital processing subsystem, a hardware/software design strategy has been followed based on a platform-based design methodology [4]. This approach addresses the development of the IPs in an integrated manner, both in the hardware domain and in the development of the APIs required for their use from the processing system. The use of the available Zynq device ecosystem facilitates the adoption of this methodology. A mixed methodology has been used for the design of the IP blocks, either using high-level synthesis, RTL design using Verilog or reusing third-party IPs (Xilinx and Analog Devices). All this set of IPs are integrated to conform the starting platform that, through incremental development processes, has allowed the incorporation of the final functionality. Some aspects of the final platform have been adjusted at RTL level.

The system performs the following tasks for processing the Digital samples (Fig.3): (1) interprets the data generated by the A/D converters; (2) add real-time stamp to the captured samples; (3) average the captured samples by a user-defined factor; (4) store the processed samples in FPGA memory, (5) save the processed samples in data files; (6) transfer the processed sample files to a server via Ethernet.

It starts with an initial configuration of the module (e.g.: turn on the UPS, set the amplification factors to 1 (0dB), set the ADCs in PIN mode, set it to average every 4 samples, etc.);

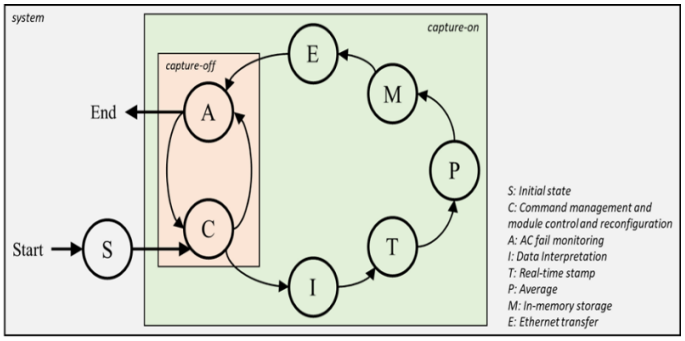

Figure 3. Task scheduling of the FPGA SoC

enters in a loop of module control and reconfiguration commands management (C) and AC fail supervision (A) (capture off loop). In case of "capture enable" the system performs the sample processing (capture on loop).

Fig. 4 shows the System-on-Chip FPGA architecture diagram of the system already defined. In the hardware domain (PL), the module control and configuration and sample processing IPs are isolated, including the following: (1) UPS Control; (2) Analog Gain Control; (3) ADCs PIN Mode Control; (4) ADCs SPI Mode Control; (5) Master/Slave Configuration; (6) AD7768 Data Interface; (7) Time Stamp; (8) Average Calculation; (9) DMA; (10) Real Time Clock (RTC) I2C Controller; (11) AXI Interconnect; and (12) PS7 Processing System.

The Processing System (software domain), run an standalone application to perform the following operations to configure the IPs that make up the hardware platform both to control and configure the DAS module and to configure the digital signal processing: (1) turn on-off the UPS and monitor the status of the external power supply; (2) select the analog gains; (3) configure the AD7768 ADCs in PIN or SPI mode, as

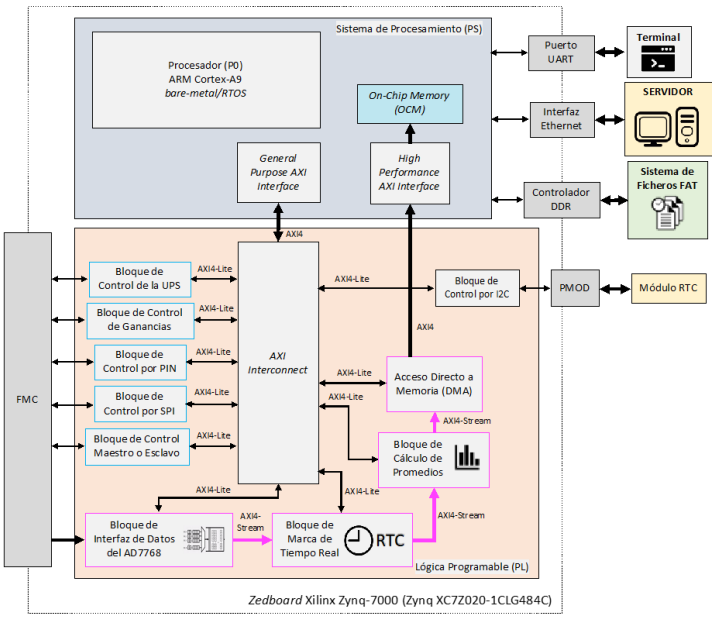

Figure 4. SoC Architecture of DAS

well as to synchronize both ADCs; (4) define the first converter of the adaptation board as master or slave; (5) read the date and time with seconds resolution from an external RTC module; (6) configure the AD7768 Data Interface to correctly read the digital signals from ADCs; (7) configure the Time Stamp IP with the real-time stamp to be added to the samples; (8), configure the Average IP with the number of samples to be processed; (9) control the DMA to store the processed samples in OCM; (10) save the processed samples in data files by means of a FAT File System (FFS) mounted in the DRR3 on board memory; (11) send these data files to a server via TCP/IP using TFTP protocol; and, read the commands received and send messages to the user using an UART port.

IV. FPGA IMPLEMETATION

Fig. 5 shows the connection of the data processing blocks. This chain of IPs allows the processing of up to sixteen simultaneous capture channels. The AD7768 Interface IP inputs are externalized to the FMC pins dedicated to the converter outputs to allow the entry of the data generated by the ADCs to the hardware. The clock signal from the ADCs must synchronize both the AD7768 Interfaces and the slave interface of the IP FIFO dedicated to the clock domain crossing. The system uses a main clock with a frequency of 100 MHz. Fig. 6 shows the storage chain, where data from Average IP is stored in OCM memory using the DMA and PS blocks. The resource utilization and power consumption are presented in fig. 7 and fig. 8 respectively. The most used resource is BRAM, used to implement internal FIFOs for data acquisition, DMA and I/O controllers (SPI, I2C, GPIO). The device has free resources to implements or increase the internal functionality using hardware resources.

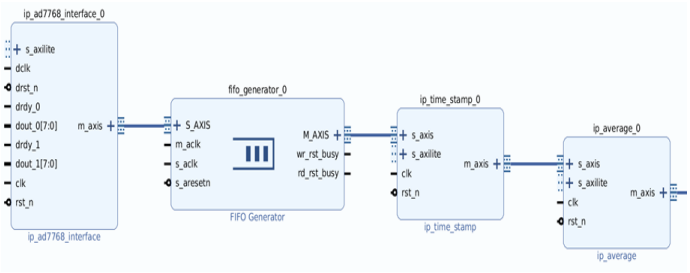

Figure 5. Data processing subsystem

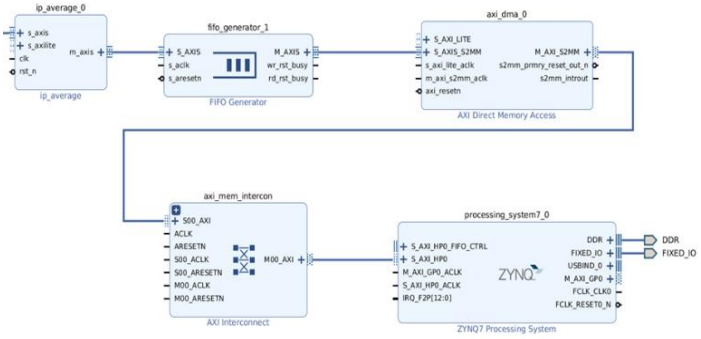

Figure 6. Data storage subsystem

Resource	Utilization	Available	Utilization %
LUT	12159	53200	22.86
LUTRAM	521	17400	2.99
FF	20861	106400	19.61
BRAM	73.50	140	52.50
IO	65	200	32.50

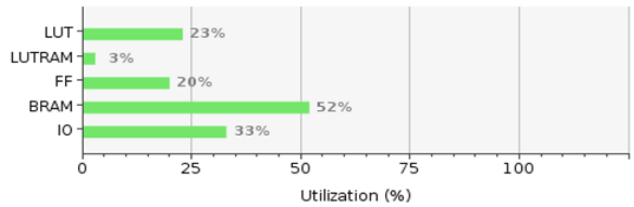

Figure 7. SoC FPGA resource utilization

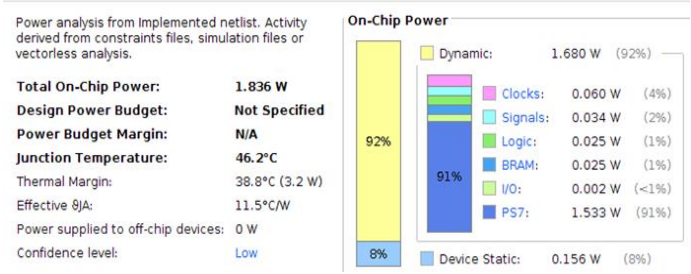

Figure 8. Power disipation of the implemented design on Zynq SoC

V. EMBEDDED SOFTWARE DESIGN

A set of C/C++ libraries for ARM Cortex A9 have been designed and/or reused to support the baremetal operation that allows the development of the main application. Table 1 shows the main libraries used and their functionality.

TABLE I. LIBRARIES FOR STANDALONE APP

System/Drivers/app	Libraries
System	xparameters.h, xil_io.h, xil_types.h, xil_printf.h, xstatus.h xtime_l.h, xstatus.h
Drivers	xgpio.h, xaxidma.h, xuartps_hw.h, PmodRTCC.h, axiqspi.h xilffs.h lwip211.h
App	menu.h, deepspace.h

VI. DESIGN VALIDATION

The System-on-Chip design has been validated on the Zedboard prototyping board, using the following validation tests: (1) SoC initialization and configuration; (2) DAS module start-up and configuration; (3) signal acquisition and processing; (4) AC fail supervision; and (5) global system validation. Fig. 9 shows the setup used for capturing and digital signal processing test using external digital pattern generator (Digilent Analog Discovery 2 [5]). The generators provide input data and synchronization to emulate the I/O of ADCs (Fig. 10). During the validation process, the content of memory has been observed and validated and the output data has been validated in console output.

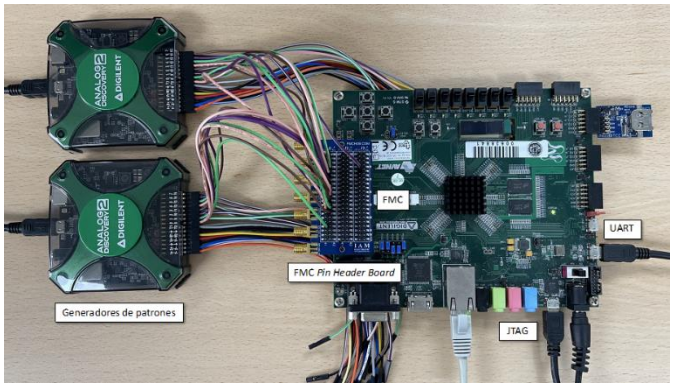

Figure 9. Setup for Data adqusition and processing validation

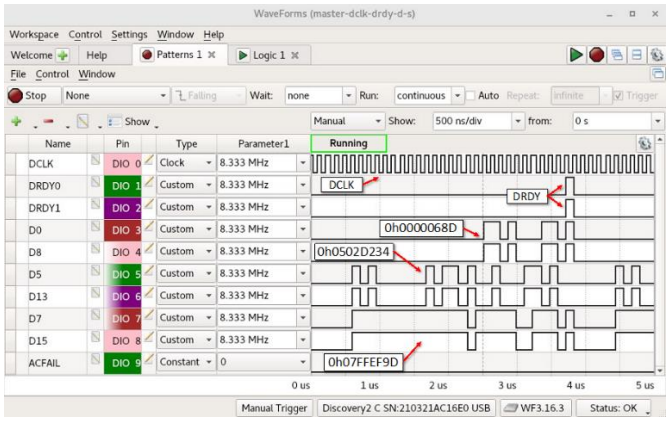

Figure 10. Signal generation for data adqusition and processing validation

Finally, the complete design has been validated over real hardware (Fig. 11) using and analog signal generator connected to the instrument input (Fig. 12). Data is captured in files and the postprocessing of the files show the results in console, including channel information, timestamp and signal value (Fig. 13).

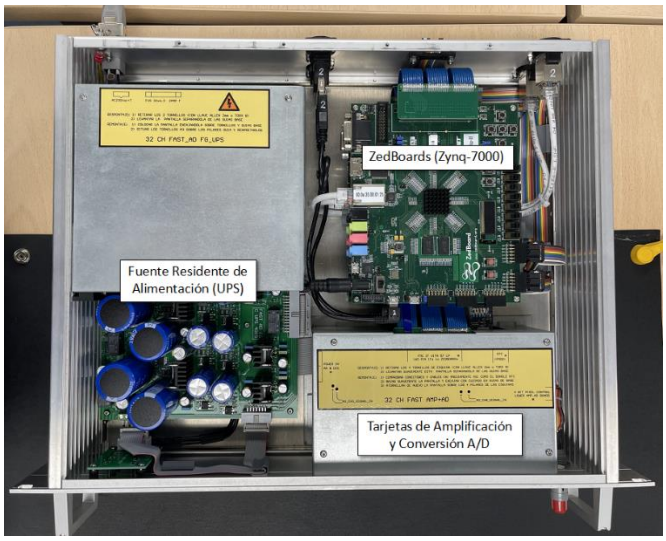

Figure 11. Final validation over real equipment

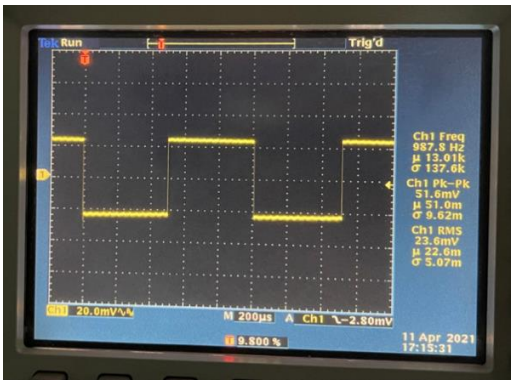

Figure 12. Analog signal generation

```
vlsiws20:~/tfm-smedina$ ./capture-value.csh 13
CH[13] TS[Thu 2022-06-30 16:40:49 185] DV[+4.732941 V]
CH[13] TS[Thu 2022-06-30 16:40:49 185] DV[+4.732219 V]
CH[13] TS[Thu 2022-06-30 16:40:49 185] DV[+4.732521 V]
CH[13] TS[Thu 2022-06-30 16:40:49 185] DV[+4.732251 V]
CH[13] TS[Thu 2022-06-30 16:40:49 185] DV[+4.735789 V]
CH[13] TS[Thu 2022-06-30 16:40:49 185] DV[+4.716495 V]
CH[13] TS[Thu 2022-06-30 16:40:49 185] DV[-2.942200 V]
CH[13] TS[Thu 2022-06-30 16:40:49 185] DV[-4.668892 V]
CH[13] TS[Thu 2022-06-30 16:40:49 185] DV[-4.673990 V]
```

Figure 13. Extract of the captured data, including Timestamp information

VII. Conclussions and Future Work

With respect to the FPGA SoC solution developed, it can acquire and processing up to sixteen digital signals simultaneously with a moderate power consumption and that allows controlling and configuring a DAS module. This SoC integrated in the DAS module provides a sixteen-channel simultaneous DAS that amplifies with different gains, captures at high speed (256KSPS) and with a resolution of 24 bits, adds Unix real-time stamps with seconds or milliseconds resolution to the samples, calculates the average of the samples and sends to a remote storage server through Ethernet the processed signals in data file format. The system can be controlled and configured by means of commands and a configuration menu (e.g.: control the capture, select the amplification gains of the signals, put the desired channels in standby, turn the equipment on or off, etc.) and stops in a controlled manner in case of power failure.

VIII. References

[1] Instituto de Astrofísica de Canarias (IAC), 'QUIJOTE CMB Experiment. Brief Description. ', *Anisotropías del Fondo Cósmico de Microondas*, 2021. [Online]. Available: http://research.iac.es/proyecto/cmb/pages/en/quijote-cmb-experiment/description.php. [Accessed: 12-Aug-2021].

[2] Analog Devices, 'Data Sheet AD7768/AD7768-4 | 8-/4-Channel, 24-Bit, Simultaneous Sampling ADCs with Power Scaling, 110.8 kHz BW', 2017.

[3] Xilinx, 'Zynq-7000 SoC Data Sheet: Overview', vol. 190, pp. 1–25, 2018.

[4] P. Marwedel, 'Application Mapping', in *Embedded System Design: Embedded Systems Foundations of Cyber-Physical Systems, and the Internet of Things*, Cham: Springer International Publishing, 2021, pp. 295–348.

[5] Digilent | Mouser, 'Analog Discovery 2', 2021. [Online]. Available: https://www.mouser.es/new/digilent/digilent-analog-discovery-2/?gclid=EAIaIQobChMIy8-k6I3B9AIVSZJmAh2H5gGWEAAYAiAAEgLYQfD_BwE. [Accessed: 30-Nov-2021].