Development of a High-Performance CCSDS 121.0-B-3 Compliant Hardware Architecture for Data Compression

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***Abstract*—As satellites increase their acquisition capabilities, their data processing requirements are growing exponentially. This project aims to develop a CCSDS 121.0-B-3 compliant data compression architecture that processes data streams of up to 8 Gbps.**

I. Introduction

Earth Observation (EO) satellites generate an increasing amount of data, which has led on-board data management systems to become a critical part of space missions [1]. This is due to the constant improvement in sensors resolution and data rate [2], as well as the growing number of sensors embarked on satellites. As a result of this growth in the amount of data to be handled, data processing and compression systems become mandatory in order to achieve a more efficient on-board storage of the satellite information [3], as well as for optimizing the transmissions of the acquired information.

In this project, a high-performance CCSDS 121.0-B-3 data compressor has been developed, verified and synthesized. Starting from the basis of the SHyLoC 3.0 compressor [4], a highly parallelized architecture has been designed and described in VHDL, in which an operation-based control allows the effective coordination of the different independent processing pipelines. The design has been successfully verified through two different verification campaigns. Once verified, the design has been synthesised and optimized, as some problems related to critical paths appeared during the first synthesis runs. After introducing some changes in the pipeline, acceptable results were finally achieved, considering project objectives.

The rest of the article is organized as follows. Section II provides an overview of the CCSDS 121 data compression standard. Next, Section III introduces the SHyLoC compression IP cores and then a detailed explanation of the proposed solution is offered in Section IV. Finally, the main conclusions of this work are summarized in Section V.

II. CCSDS 121 data compression standard

The CCSDS 121 standard specifies a universal data compressor based on Rice coding. This means that any kind of data collected on the satellite from different sources can be compressed just with a single processing core. This project aims to implement the latest version of the standard, CCSDS 121.0-B-3 [5]. The compressor defined in the standard consists of two well differentiated stages: a preprocessor and a block-adaptive encoder. The main objective of the preprocessor is to reduce the overall entropy of consecutive samples, leading the system to achieve higher compression ratios, but without necessarily reducing their size. On the other hand, the block-adaptive encoder is responsible of computing the variable length codes, which are unique for each data block of J samples (user-defined parameter) coming from the preprocessing stage. This block features a number of different options, each of which is optimal for certain input data block. The encoder is able to detect for each block which of the encoding techniques, which are simultaneously computed, is the optimal one, reaching the highest possible compression ratio. Each individual group of coded samples is known as a Coded Data Set (CDS).

III. SHyLoC IP Cores

The SHyLoC IP Cores [4] are two independent compressors, which implement the CCSDS 121.0-B-3 and CCSDS 123.0-B-1 standards. These two IPs can work in a completely autonomous manner, but they are designed to use compatible interfaces, allowing hardware designers to implement certain parts from each of them to work joinly (i.e., the CCSDS 123 predictor together with the CCSDS 121 block-adaptive encoder). The SHyLoC CCSDS121-IP, which implements both the Unit-Delay Predictor and the Block-Adaptive Encoder, is the starting point of this project, which aims to modify its sequential architecture to achieve a high-performance design for real-time data compression on-board next-generation satellites.

IV. Proposed solution

In order to be able to process bitstreams at higher data rates, a highly parallelized architecture, in which all the components specified in the standard are replicated as shown in Fig. 1, is developed in VHDL, verified and implemented.

The design receives 4 samples per clock cycle through an AXI4-Stream input interface, which are processed simultane-

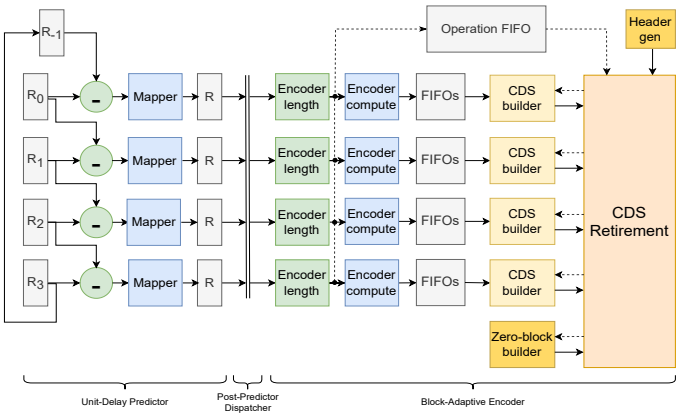

Fig. 1. Parallelized Compressor Architecture

ously by individual Unit-Delay predictors. Sample size is fixed at 16 bits, although this can be configured at compile-time.

Once the 4 samples have been preprocessed, these are internally dispatched to one of the 4 processing chains. This design fixes the J parameter to 8, meaning that each encoding chain sequentially processes blocks of 8 preprocessed samples. The internal post-predictor dispatcher is responsible for accumulating preprocessed samples during two consecutive cycles, a whole block of mapped residuals, and for forwarding it to the expected processing lane.

The block-adaptive encoders work independently of each other, except when processing those blocks requiring the *zero-block* encoding option. The *zero-block* computation differs drastically from any of the other encoding techniques as it introduces dependencies between an undetermined number of consecutive all-zeros blocks. If no additional mechanisms are introduced, then it implies to break the autonomous scheme of the encoding parallel chains, thus complicating not only the control but also the datapath, as these may be injected at the output at any time from an independent block-adaptive encoder.

A major change that was introduced in the parallelized design is the implementation of an operation-based control, which radically differs from the flow-based SHyLoC control. The operation-based control allows to write the CDSes into the output bitstream in a completely controlled order, thanks to the use of unique auto-incremental identifiers that are assigned to the blocks of data as these are received from the predictor. This control scheme also eases the generation of Zero-Block CDS, as this process can be controlled in a centralized manner. Each block of samples has its corresponding operation, which is completed once its CDS is written into the output bitstream.

The format of a CDS depends directly on the codification technique used, as well as on whether it includes a reference sample or not. A number of consecutive CDS, which come from different encoding chains, are grouped in the final dispatcher, which also appends the header and sends the whole bitstream through the output interface, also implemented with an AXI4-Stream protocol.

Please note that this design, which consists of 4 parallel processing chains, can be easily scaled to a more parallelized variant, which would ultimately allow to process even at higher data rates.

A. Verification and Synthesis Results

A set of testbenches were developed to specifically verify the predictor and the internal dispatcher. Once the system was fully integrated, the most extensive verification phase started. A general testbench that checks for the correctness of the compressed bitstream by comparing this with its corresponding reference bitstream, previously generated using a reference software, was developed. This extensive verification allowed to thoroughly test the design at various levels, thanks to the usage of different testcases.

Once extensively verified, the design was synthesized. The selected target FPGA is the Xilinx Kintex Ultrascale XCKU040. Some initial synthesis allowed us to detect a critical path that seriously limited the final performance. After applying additional pipelining, reasonable area and timing results were achieved, which are summarized in Table I. The final throughput is estimated at **7.776 Gbps**.

TABLE I
SYNTHESIS RESULTS

Resource	Result	Utilization (%)
System clock	121.5 MHz	-
I/O Ports	378	-
I/O Register Bits	0	-
Block RAMs	0	0
LUTs	28329	11.68
Non I/O Register Bits	8774	1.80
Ultra RAMs	0	0
DSP48s	4	0.2

V. CONCLUSION

This project consisted in the development of a high-performance CCSDS 121.0-B-3 data compressor, which is able to handle input data streams of up to 8 Gbps. The SHyLoC CCSDS121-IP data compressor was taken as the starting point of this architecture, and its internal components were replicated to process more than 1 sample per clock cycle. The design has been successfully verified and synthesized, ultimately achieving adequate values regarding hardware occupancy and operation frequency.

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