Analysis and Design of a Digital Beamformer for LEO Satellite Constellations

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***Abstract*— The objective of this research is the design of a digital beamforming algorithm using MATLAB/Simulink. Subsequently, the algorithm will be implemented on an Field Programming Gate Array (FPGA). Performance comparison between the results obtained from the performance model and those described in the MATLAB code will be conducted. Finally, the Hardware Description Language (HDL) code will be generated via Simulink and verified through a testbench. From this code, the Intelectual Property (IP) block is generated, necessary for its implementation in Vivado.**

Keywords-component: array; beamforming; Delay-and-Sum;

I. INTRODUCTION

Low Earth Orbit (LEO) satellite constellations are a set of low-Earth orbiting satellites that work cooperatively and orbit relatively close to the Earth's surface at altitudes below 2000 km. They offer reduced time delay in data transmission, which is crucial for real-time applications such as videoconferencing and meteorological data acquisition [1].

When antennas are grouped together, forming an array, their properties depend on the geometrical arrangement and the number of antennas [2]. Beamforming techniques are essential in satellite communications for efficient pointing from the earth's surface to a satellite, typically using phased arrays.

II. BEAMFORMING ARCHITECTURES

Beamforming is a technique used in communications systems to enhance both the direction and strength of the transmitted or received signal. It allows focusing the energy of a signal in a specific direction, improving the efficiency and quality of transmission or reception in the face of limiting factors such as attenuation or the presence of interference and noise.

A. Analog beamformer

An analog beamformer controls antenna beamforming and beam direction by manipulating the phases and amplitudes of the feed signals using components like delay networks, power dividers, variable gain amplifiers, and phase shifters. This combination produces the desired radiation pattern [3].

B. Digital beamformer

A digital beamformer digitizes the received signal for further processing to achieve the desired radiation beam. This approach has two main features. First, the total available information is preserved, expressed as N single-element signals as opposed to the generation of an analog signal, which operates with a single signal. Secondly, once the input analog signals are correctly digitized, they can be manipulated indefinitely without adding further errors, since the digital representation of the signal is used instead of the actual magnitude of the received signal [4].

C. Hybrid beamformer

A hybrid beamformer combines both analog and digital components in its design. This allows taking advantage of both technologies, providing a balance between the flexibility and efficiency of digital solutions and the simplicity and low cost of analog solutions. In these systems, analog components are used for signal preprocessing at each antenna and extensive signal processing in digital format [5].

III. DESIGN

The development of the beamformer in Simulink is presented. A comparison is carried out between a model based on a MATLAB algorithm. The design process includes efficient data processing techniques, meeting design constraints for HDL code generation, and comparing results from the MATLAB code and Field Programming Gate Array (FPGA) implementation.

A. Delay and sum algorithm

This technique employs a delay and amplitude weighting at the output of each antenna and then combines the resulting signals. The delays are selected so as to maximize the sensitivity of the array to signals coming from a specific direction. By adjusting these delays, the direction in which the antenna array is focused or pointed (source) can be oriented, and the waveforms captured by the different antennas are combined in a constructive manner [6].

It should be noted that this algorithm is quite important in the design of this project because, if it were not used, the same receive signal could not be obtained. By employing delay arrays to spatially steer the direction of the antenna array, it is observed that, if its orientation direction coincides with that of a radiation source, the output power is maximized.

B. Beamforming algorithm in MATLAB

The functional phase-shifting beamformer algorithm has been implemented in a Hardware Descriptiom Language (HDL) algorithm subsystem, using Simulink blocks for HDL code generation. The beamformer performs calculations of the required phase for each of the ten channels, with the objective of maximizing the received signal power along the angle of incidence. (Figure 1)

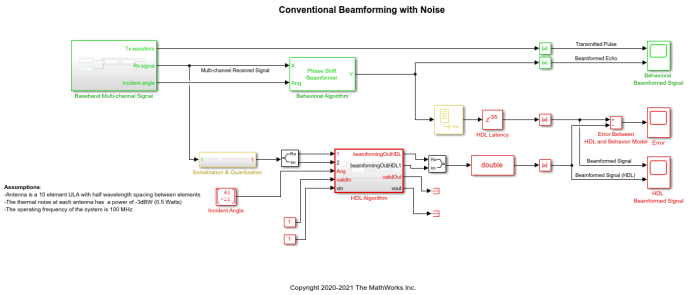

Figure 1: Simulink model with the operational and implementation algorithms.

The algorithm used in this comparison is a phase-shifted beamformer using delays, which calculates the necessary phase adjustments for each channel to maximize the received signal power in the incident angle direction. This algorithm is implemented both in the model described in MATLAB code and in the HDL model to allow a direct comparison of their results. By analyzing the plots obtained by simulating the design it is possible to evaluate the performance and accuracy of the HDL implementation compared to the model described in MATLAB code, ensuring that the FPGA-based beamformer performs as intended.

C. Results

Figure 2 represents examples of the results in the Questa Sim and Simulink scopes. It shows both the co-simulation and the HDL model producing a 79 ms delayed version of the original signal produced by the model described in MATLAB code, as expected, with no difference between the two waveforms. The delay is due to the original delay added in the Algorithm subsystem and an additional delay due to the delay balancing added by the HDL code generation.

IV. BLOCK DESIGN

Once this process has been completed, the block design implemented in Vivado is opened.

The design runs within Vivado show the area consumption expressed in LookUp Table (LUT), Flip-Flops (FF), Block RAM (BRAM), UltraRAM (URAM) and Digital Signal Processor (DSP).

The "On-Chip Power" graph (Figure 3) shows the distribution of power consumption among the various components of the design, which helps to identify which areas of the design consume the most power.

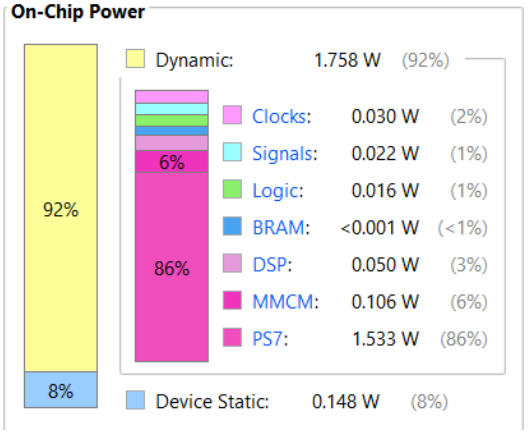

Figure 2: On-Chip Power

V. CONCLUSIONS

This research outlines the workflow for developing a beamformer in Simulink for FPGA implementation, emphasizing the importance of comparing implementation model results with MATLAB code models. The HDL code generated and verified through a testbench, and the block design is implemented, demonstratimg that the digital beamformer can be effectively implemented on an FPGA.

In the first part, the workflow required to develop a beamformer in Simulink for FPGA implementation is described, highlighting the importance of comparing the results of the implementation model with the model described in MATLAB code.

In the second part, the HDL code is generated and verified from the designed model. A testbench is used for the verification of this code. The co-simulation process for verification through a testbench is described. In addition, a block design is created and verified in Vivado. The syntesis is carried out, checking the FPGA resources used.

REFERENCES

[1] Z. Qu, G. Zhang, H. Cao, and J. Xie, “LEO Satellite Constellation for Internet of Things,” IEEE Access, vol. 5, pp. 18391–18401, Aug. 2017, doi: 10.1109/ACCESS.2017.2735988.

[2] C. A. Balanis, Antenna theory: analysis and design. John wiley & sons, 2016.

[3] M. Q. Abdalrazak, A. H. Majeed, and R. A. Abd-Alhameed, “A Critical Examination of the Beam-Squinting Effect in Broadband Mobile Communication: Review Paper,” Electronics (Basel), vol. 12, no. 2, p. 400, Jan. 2023, doi: 10.3390/electronics12020400.

[4] A. M. Dixit et al., “A CMOS Digital Beamforming Receiver,” Anal Biochem, vol. 11, no. 1, pp. 1–5, 2018.

[5] B. Chandhoke, S. Product, and L. Manager, “Design innovations in 5G mmWave FEMs & phased arrays”.

[6] J. Grythe, “Beamforming algorithms-beamformers.”