Design of a K/Ka-band Low Noise Amplifier for 5G Receivers in a 45-nm SOI Technology

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***Abstract*— This paper presents the implementation of a low-noise-amplifier (LNA) with an operating frequency of 30 GHz for a 5G receiver. The LNA is designed in a GlobalFoundries technology named 45RFSOI, with minimum gate length of 45 nm. The LNA is implemented in a cascode configuration with source degeneration. The cascode benefits from enhanced I/O isolation, wideband response, high gain and low power, whereas source degeneration enhances noise figure (NF) and device stability and brings S_{11} closer to S_{opt}. The design procedure consists of finding the optimal current density J_{DS} for low-noise operation, with reasonable gain and low-power consumption. Post-layout EM simulations are presented, as well as Monte Carlo results, demonstrating a gain of 15.9 dB and a NF of 2 dB, with a power consumption of only 9 mW.**

Keywords– Low Noise Amplifier (LNA), 45RFSOI, 5G Receiver, Cascode, Common-Gate (CG), Common-Source (CS), Layout, Electromagnetic (EM), Monte Carlo.

I. INTRODUCTION

In the last decade, the sharp growth of wireless communications has generated a multitude of communication standards. As a result of wireless communications, new standards are defined for specific applications such as medical services or Smart Cities. For this reason, manufacturers and designers adopt specific design techniques such as reducing the power consumption of devices to improve their efficiency. For this reason, 5G technologies emerge as a combination of predecessor wireless communication technologies such as 2G, 3G, 4G or IEEE 802.11 standards [1].

This paper describes the design and implementation of a K/Ka-band low-noise amplifier for a 5G receiver using the 45RFSOI technology. The LNA architecture is discussed in Section II. Simulation results of the implemented circuit are summarized in Section III. Finally, in Section IV, conclusions are drawn.

II. PROPOSED LNA ARCHITECTURE

The proposed LNA is part of the receiver front-end of a K/Ka-band 5G transceiver. It is the first element in the signal path and, therefore, it is essential that the signal is amplified by introducing a noise as low as possible. In addition, there must be reasonable impedance matching between the antenna and the amplifier itself to avoid reflection losses at the input. Therefore, it is necessary that the LNA complies with two fundamental characteristics: unconditional stability and a high linearity to avoid signal distortion. The topology chosen is the cascode, which is formed by a common-source (CS) amplifier in series with a common-gate (CG) transistor, as shown in Figure 1 (M_{CS}, M_{CG}). The reasons for choosing this topology are the improvements in the I/O isolation, the achievement of a high bandwidth, increased gain, greater stability and current reuse, highlighting these aspects compared to other solutions [2].

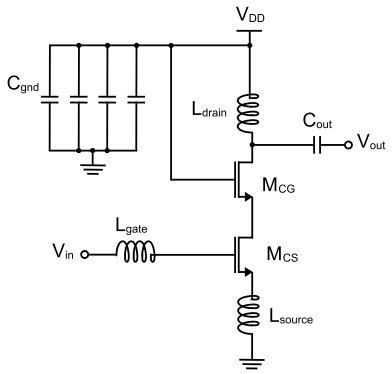

Figure 1. Proposed cascode LNA schematic.

The topology of the proposed LNA is shown in Figure 1. At the top right of the circuit, named V_{DD}, is the power supply, which is initially set to 900 mV. Also, there are three inductances, named L_{drain}, L_{gate} and L_{source}, respectively, as well as an output capacitor, named C_{out}, used to match the output impedance of the LNA to 50 Ohm. In the center of the Figure, two transistors are shown, in CG and CS configuration, respectively. The input and output terminals used to perform simulations are located at the ends (V_{in} and V_{out}). Furthermore, at the input of the circuit, an external capacitor is used with an RF choke, which are used to couple the AC input signal and bias the gate of M_{CS}. Finally, four capacitors are connected in parallel to the power supply, whose function is to ensure that the gate of transistor M2 is grounded in AC to prevent the circuit from becoming unstable and filter power supply noise.

At the schematic level, two designs are developed. First, an ideal-component LNA is developed, whose function is to obtain the initial proof-of-concept performance of the circuit. The second schematic design consists of replacing the ideal components with components from the process design kit (PDK). With this second version, the results of the LNA are more accurate and realistic, obtaining a gain of 16.5 dB and a NF of 1.7 dB, keeping a power consumption of 9 mW. As a result of the schematic design, the transistors dimensions selected are a total width (w_T) of 50 µm, a number of fingers (*nf*) of 50 and a gate length of 40 nm. Furthermore, L_{gate} has an inductance of 130 pH, L_{source} is 119.9 pH and L_{drain} is 477.9 pH. Meanwhile, C_{out} is equal to 26.8 fF. For the input (S_{11}) and output (S_{22}) return losses, values of –14.2 dB and –19.5 dB are achieved, respectively. Finally, the stability factor is 1.291.

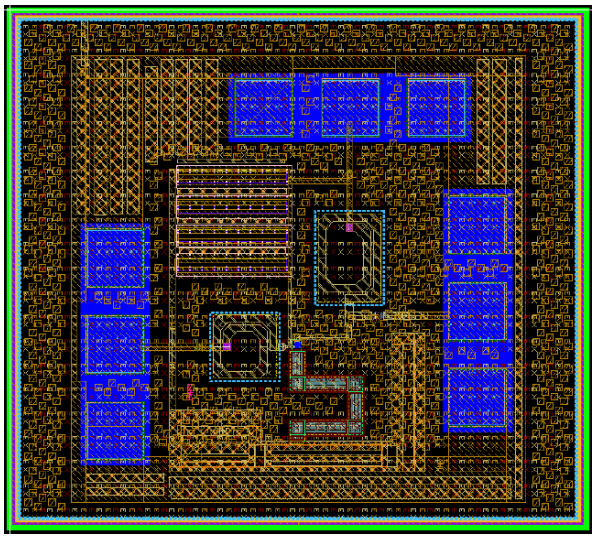

Figure 2. Layout of the proposed LNA.

III. Simulation Results

The next step is to implement the LNA layout. The Cadence Virtuoso Layout XL tool and the 45RFSOI models proposed by the foundry are used for this purpose. The result of this process is presented in Figure 2. Post-layout simulations of the proposed LNA were performed using Spectre RF software. The LNA has a total area of 900 µm × 1 mm, including pads. In addition, simulations are performed with the ElectroMagnetic eXtraction software (EMX) models of the input matching, output matching, source degeneration and cascode gate networks. After including these models, a gain of 14.8 dB and a noise figure of 1.9 dB are obtained, with the input and output matching centered at the desired working frequency of 30 GHz.

To obtain an estimation of the performance that the LNA can provide, a Monte Carlo analysis is used, and the behavior of the circuit is studied. The Monte Carlo analysis consists of a stochastic procedure that submits the LNA to 250 random samples. Then, the mean and standard deviation of the most relevant circuit performance metrics such as gain, stability, S_{11}, S_{22} or NF can be derived [3]. Inside the Virtuoso design environment, this analysis can be configured to study the most important LNA features such as S_{11}, S_{22}, gain and NF. The mean value of S_{11} is –12.7 dB, with a maximum value of –5 dB and a minimum value of –28.4 dB. For S_{22}, a mean value of –12.4 dB is obtained, with a maximum value of –4.3 dB and a minimum value of –36.8 dB. The average gain value is 15.9 dB, with a mean value of 17.8 dB and a minimum value of 14.1 dB. And finally, the NF has a mean value of 2 dB, a maximum value of 2.1 dB and a minimum value of 1.8 dB.

IV. Conclusions

This paper presents the design of a low-noise-amplifier in 45RFSOI technology for a 5G receiver. Post-layout simulations demonstrate that the circuit is competitive in terms of area and power consumption compared to similar designs. In addition, it offers gain and noise figure performances that match other LNAs for 5G receivers, as shown in Table 1.

Table 1. Performance comparison of different LNAs

Parameters	Different LNAs			
	[4]	[5]	[6]	***This work***
Technology	45RFSOI	28 nm CMOS	22 nm FDSOI	45RFSOI
Frequency (GHz)	28	33	32.8	30
Max. Gain (dB)	24	18.6	10.2	17.8
Noise Figure (dB)	4	4.9	2.2	2
Supply (V)	1.1	1.2	1.6	0.9
Power Consumption (mW)	18.5	9.7	15	9
Area (µm^2)	150000	230000	120000	900000

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