A Packaged Synthesizer for DVB-H

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***Abstract*—This paper presents a BiCMOS synthesizer enclosed in a 16-pin QFN package for DVB-H standard. The influence of the bond-wires, ESD pads, solder dots and package in the synthesizer response is studied, showing simulations before and after the package.**

Keywords-component; DVB-H; BiCMOS; VCO; synthesizer; QFN; phase noise.

I. INTRODUCTION

In the last years, standards like DVB-H [1][2] have allowed to the users the access to TV services in handheld devices. DVB-H standard works in the IV and V UHF bands, from 470 MHz to 862 MHz. The channel separation is 8 MHz and the channel bandwidth is 7.61 MHz. The relationship between the channel center frequency and the channel number (N) is the following:

$$f_o = (470 + 4 + (N - 21)\cdot 8)\ \text{MHz}, \quad N = 21,...,69 \qquad (1)$$

This paper deals with the design of the synthesizer for a direct conversion architecture for DVB-H. In this case one Phase Locked Loop (PLL), working at the channel centre frequency, has been designed. The block diagram of the proposed synthesizer is shown in Figure 1. and it uses a classical PLL topology where the divider is composed by a fast divider and a programmable divider (dual modulus).

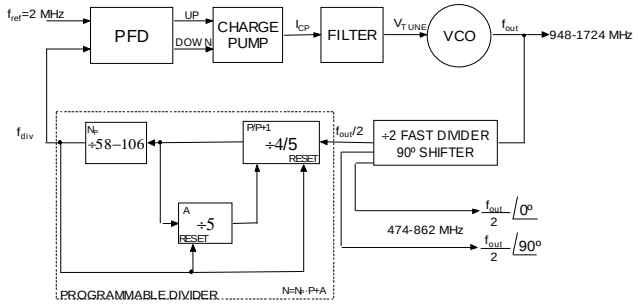

Figure 1. Synthesizer for DVB-H.

The article is organized as follows. In Section II, circuit structures which are used in the synthesizer are analyzed. Section III deals the package influence in the synthesizer performance. Synthesizer simulations are presented in section IV and finally, some conclusions are drawn in Section V.

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II. CIRCUIT STRUCTURES

A. *Phase Frequency Detector and Charge Pump*

The phase and frequency errors are detected by PFD which is a state machine with RS flip-flops as memory elements. The charge pump structure consists of a pair of current sources with switches.

B. *Filter*

The selected loop filter is a passive three-pole filter. This comprises a second order filter section and a RC section, providing an extra pole to assist the attenuation of the sidebands at multiples of the comparison frequency that may appear. Due to high capacitors values this filter is external.

C. *VCO*

It is implemented as an LC oscillator topology integrating all the components of the tank on-chip. V_{TUNE} is the VCO tuning voltage. An array of switched capacitors was used to sweep the whole frequency range, S1, S2, S3 and S4 signals control the capacitor array. To facilitate the integration of inductors and capacitors, the VCO should run at twice the required UHF frequency (from 948 MHz to 1716 MHz).

D. *Fast divider and phase shifter*

The fast divider block is composed by a CML (current mode logic) fast divider, which divides the VCO output by two as well as generates the 0º and 90º signals. The buffers are to drive the mixers and they are matched to 50 Ω. A CML to CMOS level converter is used to drive the dual modulus programmable divider.

E. *Programable divider*

The programmable divider also controls the VCO switches to select the correct sub-band, depending of the wanted output frequency. In the prototype fabrication, the programmable divider was simplified and it composed by a divider by 5 followed by programmable divider by Np (114, 130,138 and 170). With this configuration we can test at least one channel for each sub-band. It was implemented using VHSIC Hardware Description Language (VHDL).

III. PACKAGED SYNTHESIZER

The synthesizer components were integrated in 16-pin QFN (5x5mm) package with the exception of the loop filter. To simulate the packaged version of the synthesizer, pads with ESD protection, bond-wires, package and solder dots were taking into account. The design needs 11 connection pins (see Figure 2.).

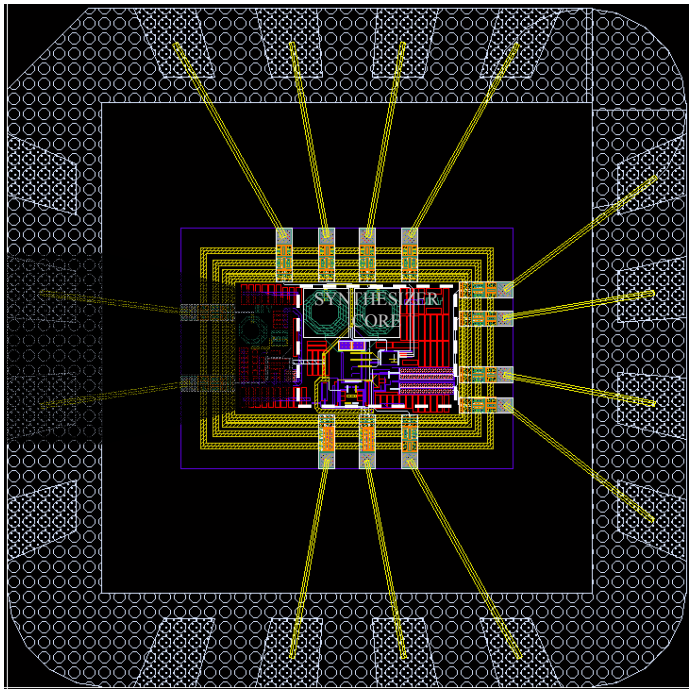

Figure 2. Synthesizer in a QFN16 package.

Figure 3. shows a post layout simulation of the synthesizer including the package effect. This simulation was very time-consuming and includes the V_{TUNE} signal, the current pulses from the charge pump (Icp), and the inputs of the PFD. As seen in Figure 3. , we can observe how V_{TUNE} voltage decreases tending to stabilize its value.

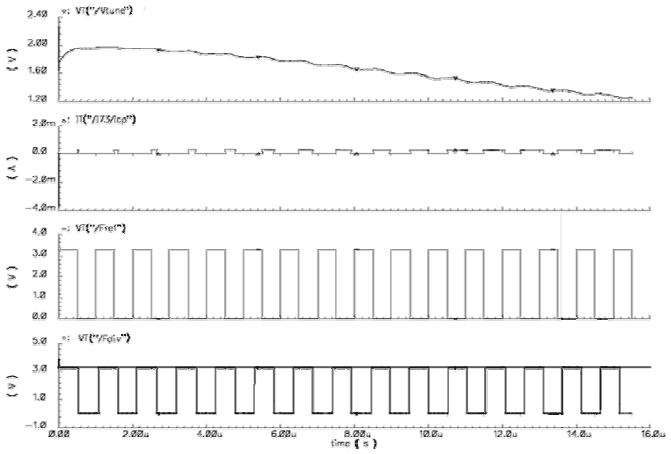

Figure 3. Post layout simulation of the synthesizer inluding package effect.

Figure 4. shows V_{TUNE} voltage post-layouts simulations without and with package effect. In the simulation with the package, we can observe a ripple in V_{TUNE} signal.

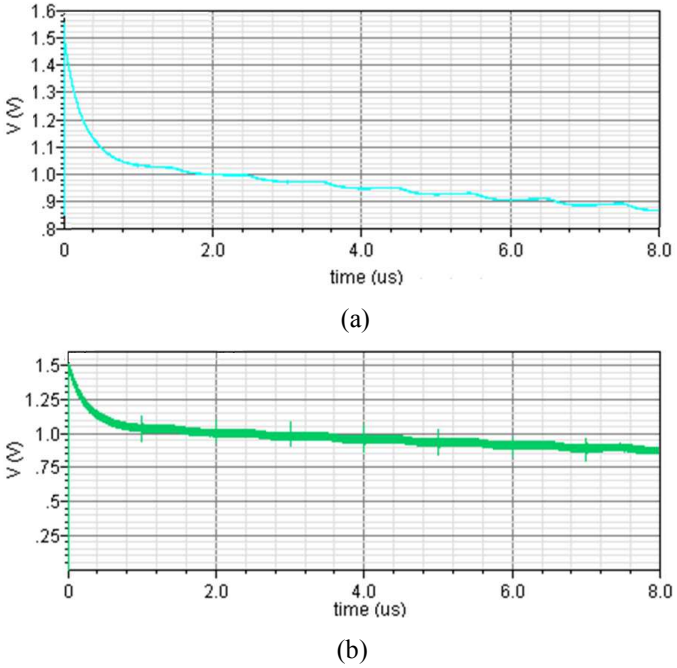

Figure 4. V_{TUNE} voltage post-layout simulatioins without (a) and with (b) package effect.

IV. CONCLUSIONS

This paper shows the design procedure of an integrated synthesizer in a 16-pin QFN package for DVB-H standard. Bond-wires, ESD pads, solder dots and package were taken into account in the synthesizer response, showing simulations after and before the packaging.

REFERENCES

[1] Guido Retz, Phil Burton, "A CMOS Up-Conversion receiver Front-End for Cable and Terrestrial DTV Applications," *IEEE Int. Solid-State Circuits Conf.,* vol. 1, pp. 442-506, Feb. 2003.

[2] Patrick Antoine, Philippe Bauser, Hugues Beaulaton, Martin Buchholz, Declan Carey, Thierry Cassagnes, T. K. Chan, Stephane Colomines, Fionn Hurley, David T. Jobling, Niall Kearney, Aidan C. Murphy, James Rock, Didier Salle, and Cao-Thong Tu, "A Direct-Conversion Receiver for DVB-H," *IEEE J. Solid-State Circuits*, vol. 40, pp. 2536-2546, Dec. 2005.

[3] S. L. Khemchandani, J. del Pino, E. López-Morillo, U. Alvarado, D. Ramos-Valido, B. Palomo, F. Muñoz-Chavero, "RF and Mixed Signal Circuits for a DVB-H Receiver," *Analog Integrated Circuits and Signal Processing*, , vol. 65, pp. 1-14, 2010.