Design and modelling of rectifiers for RFID

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***Abstract*—The objective of this work is to study the possibility of implementing SOI rectifiers for UWB RFIDs with undoped Double Gate MOSFETs (DG-MOSFETs). For that purpose we use two commercial TCAD tools, Sentaurus Device (created by Synopsys) and ADS (created by Agilent), where in a large signal circuit model derived for the transistors is implemented with Verilog-A. Once the DG-MOSFETs output characteristics are fit, the rectifier performance at high frequencies is simulated; numerical and electrical results are successfully compared.**

Keywords—SOI; RFIDs; UWB; DG-MOSFET; rectifier

I. DG-MOSFET LARGE SIGNAL CIRCUIT MODEL

The schematic of the DG-MOSFET large-signal equivalent circuit is shown in Fig. 1, and is explained as follows.

A. The DC Drain Current

The DC drain current is based on a charge control model presented in [1]. The inversion charge, Q, and drain current, I_{DS}, are calculated respectively as

$$Q = 2C_{ox}\left(-\frac{2C_{ox}\beta^2}{Q_o}+\sqrt{\left(\frac{2C_{ox}\beta^2}{Q_o}\right)^2+4\beta^2\ln^2\left[1+\exp\left(\frac{V_{gs}-V_{th}+\Delta V_{th}-V}{2\beta}\right)\right]}\right) \quad (1)$$

$$I_{ds}=\frac{W\mu}{L}\left[2\beta(Q_s-Q_d)+\frac{Q_s^2-Q_d^2}{4C_{ox}}+8\beta^2C_{Si}\ln\left(\frac{Q_d+2Q_o}{Q_s+2Q_o}\right)\right] \quad (2)$$

The resulting numerical and electrical output characteristics are compared in Fig. 4, showing a good agreement.

B. The capacitances

For a proper DG-MOSFET transient response [2], the capacitances from gate to source, C_{gs}, gate to drain, C_{gd}, and drain to source, C_{ds}, must be incorporated in the circuit model.

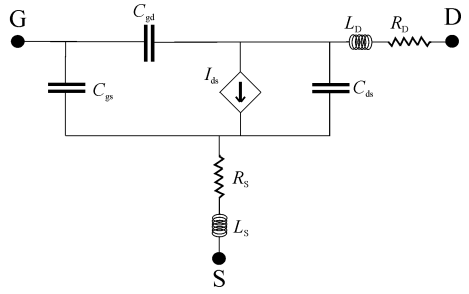

Figure 1. DG-MOSFET large-signal equivalent circuit

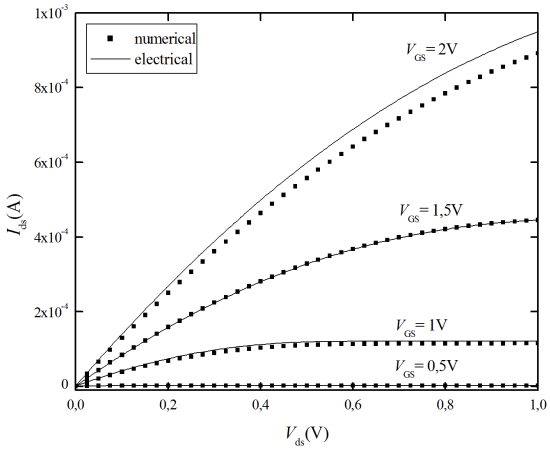

Figure 2. Numerical and electrical DG-MOSFET output characteristics

So, the capacitance C_{gs} can be written as

$$C_{gs}=\frac{\frac{W^2\mu}{I_{ds}}\left[\left(\frac{Q_s^2}{2C_{ox}}+\beta Q_s+\frac{\beta Q_s^2}{Q_s+2Q_o}\right)-\frac{Q_{Tot}}{WL}\cdot\left(2\beta+\frac{Q_s}{2C_{ox}}-\frac{8\beta^2C_{Si}}{Q_s+2Q_o}\right)\right]}{\frac{1}{2C_{ox}}+\beta\left(\frac{1}{Q_s}+\frac{1}{Q_s+2Q_o}\right)} \quad (3)$$

In a similar way for C_{gd}, and considering the symmetry of the DG-MOSFET, an identical expression to (3) is derived, replacing Q_s by Q_d

$$C_{gd}=\frac{\frac{W^2\mu}{I_{ds}}\left[\left(\frac{Q_d^2}{2C_{ox}}+\beta Q_d+\frac{\beta Q_d^2}{Q_d+2Q_o}\right)-\frac{Q_{Tot}}{WL}\cdot\left(2\beta+\frac{Q_d}{2C_{ox}}-\frac{8\beta^2C_{Si}}{Q_d+2Q_o}\right)\right]}{\frac{1}{2C_{ox}}+\beta\left(\frac{1}{Q_d}+\frac{1}{Q_d+2Q_o}\right)} \quad (4)$$

Finally, the expression of the last capacitance is

$$C_{ds}=\frac{\left(\frac{dQ_D}{dQ_S}-\frac{2W\mu Q_D}{LI_{DS}}\right)\cdot\left(2\beta+\frac{Q_d}{2C_{ox}}-\frac{8\beta^2C_{Si}}{Q_d+2Q_o}\right)}{\frac{1}{2C_{ox}}+\beta\left(\frac{1}{Q_d}+\frac{1}{Q_d+2Q_o}\right)} \quad (5)$$

II. CONVERGENCE PROBLEMS

Once the large-signal equivalent circuit of the DG-MOSFET has been introduced in ADS through Verilog-A, an industry standard modeling language for analog circuits, the resulting rectifier performance is validated with numerical simulations.

However, the electrical transient simulations are not immediate: both problems of convergence and accuracy

TABLE I. FITTING PARAMETERS FOR C_{GS} AND C_{DS}

A_{0g} (Fcm^{-2})	A_{1g}	A_{2g} (V^{-1})	A_{3g} (Fcm^{-2})
$-1.26\cdot10^{-14}$	-15.26	15.06	$1.26\cdot10^{-14}$
A_{0s} (Fcm^{-2})	A_{1s}	A_{2s} (V^{-1})	A_3 (Fcm^{-2})
$3.28\cdot10^{-14}$	-4.88	11.44	$-3.28\cdot10^{-14}$

happen, because the modeled capacitances C_{gs} and C_{ds}, expressions (3) and (5) respectively, have uncertainties around V_{ds} = 0 V, varying drastically their values when V_{ds} is very small [3]. To avoid this problem expressions (3) and (5) are approximated by sigmoidal functions (6), which are continuous, with continuous derivatives:

$$C_{\xi d}\big|_{V_{gd}=0} = \frac{A_{0\xi}}{1+e^{\left(A_{1\xi}+A_{2\xi}\cdot V_{DS}\right)}} + A_{3\xi},\ \xi \text{ with g, d} \qquad (6)$$

where the fitting parameters for C_{gs} and C_{ds}, $A_{0\xi}$, $A_{1\xi}$, $A_{2\xi}$, $A_{3\xi}$, are indicated in Table I. The goodness of this fit is shown in Fig. 3. Similar results are obtained for C_{gd}, but are not shown, because it is being neglected in the large signal circuit model.

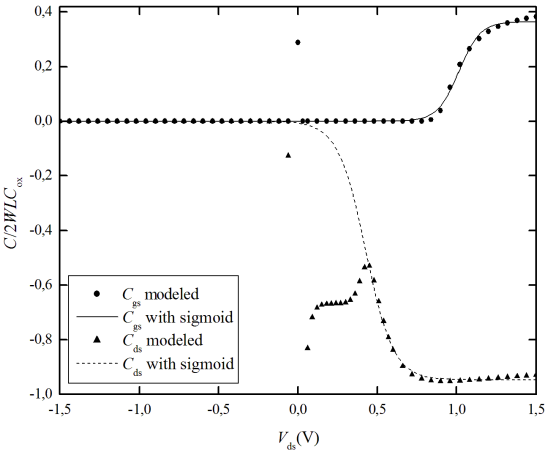

Figure 3. C_{gs} and C_{ds} and their sigmoidal aproximations

A. Results

Once the rectifier has been successfully simulated with ADS, the rectified signal must be compared with that obtained with Sentaurus Device. We have obtained the output voltage of both simulations, varying the power of the input signal. The result is shown in Fig. 4, where the output voltage is evaluated as the average value, when reaching the steady state. A good agreement between numerical and electrical results is achieved. Fig. 5 compares the electrical rectified voltage of our rectifier at 5GHz, with another one implemented with commercial Texas Instruments N-MOSFETs, with identical dimensions: A similar DC output voltage is obtained with DG-MOSFETs and Texas Instruments N-MOSFETs: 0.6 V. It is remarkable to note that the threshold voltage of the Texas Instruments transistor (0.37 V) is 0.18 V lower than that of the DG-MOSFET (0.55 V). Therefore, using appropriate metal gates in the DG-MOSFET be achieved. As Figure 5 indicates using TiN, wich work function is 4.2 eV [5], the DC rectified voltage with DG-MOSFET grows up to 0.85 V.

Finally, we study the influence of the number of stages on

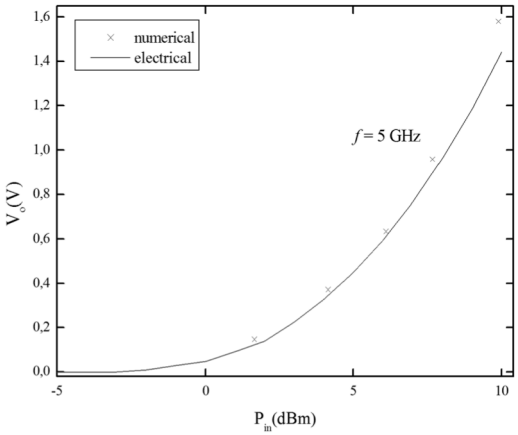

Figure 4. Numerical and modeled rectified output voltage *vs.* input power

the output voltage of the rectifier. Figure 6 shows the output voltage, when varying the input power, for different number of stages: from one to five. Notice than up to two stages the output voltage increases, and for higher values it starts decreasing. Therefore, the optimal number of stages in the rectifier with DG-MOSFETs is two. The way to connect different basic cells is described in Figure 7. Here is represented a two stages rectifier schematic in ADS. It can be observed that the input stages are connected in parallel and the outputs are connected in serial. This allows increase the final output voltage as the sum of the each individual output voltage rectified belongs to each stage.

This result is in contrast with the found in [6] with conventional N-MOSFETs, where six stages were optimal. Thus, when using DG-MOSFETs, less number of stages is expected to achieve the optimal performance of rectifiers.

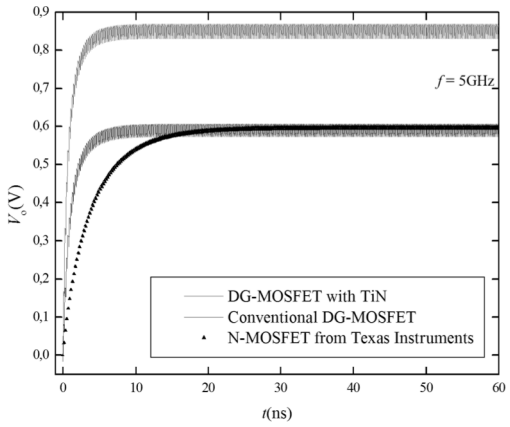

Figure 5. Rectified DC output voltage with DG-MOSFETs in ADS (solid line), and N-MOSFETs from Texas Instruments (dotted line) for an input power of 5 dBm at 5 GHz, and a load resistance of 10 kΩ

III. SHORT CHANEL EFFECTS

Once the length channel starts to decrease the different short channel effects have to be considered in the device [4], as saturation velocity and the effective mobility among others. In Fig. 8 it can see the varying ΔL with V_{ds} and how decreases while V_{gs} increases.

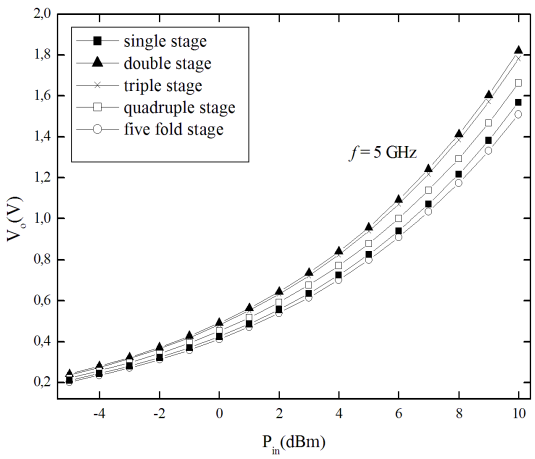

Figure 6. Modeled rectified output voltage for multiple stage configurations, using TiN, are compared.

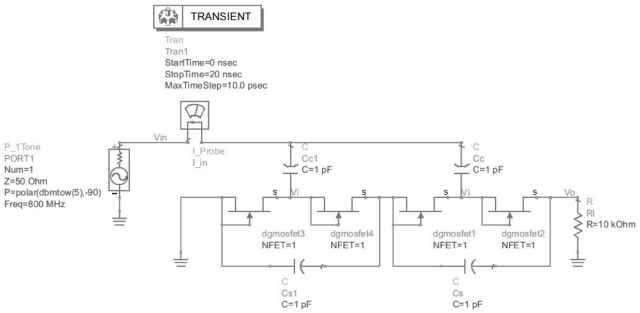

Figure 7. DG-MOSFET Rectifier with two stages implemented in ADS

In the Fig. 9 it can observed a comparison between modeled and numerical drain current, now considering SCE, that increase the drain current.

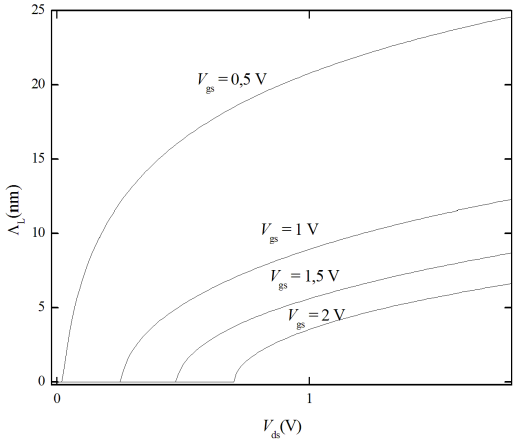

Figure 8. ΔL based on V_{ds} for different values of V_{gs}

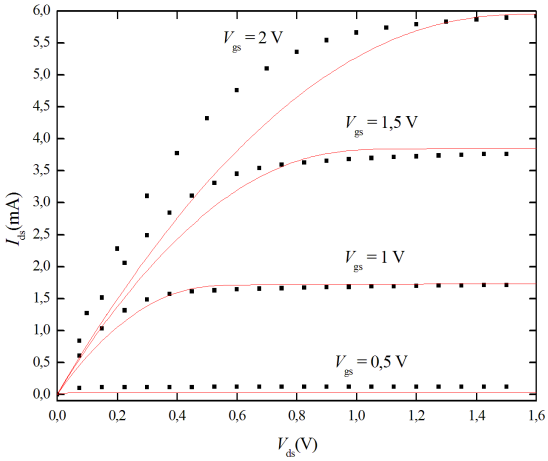

Figure 9. I_{ds} based on V_{ds} for different values of V_{gs}

IV. CONCLUSIONS

This work validates the SOI technology to design RFIDs in UWB. Using compact models of DG-MOSFETs, implemented in ADS with Verilog-A, RFID rectifiers have been electrically simulated, validating the results with numerical simulations.

For different transient simulations, it has been observed that for the frequency range covered by the UWB, the proposal rectifier with DG-MOSFETs efficiently rectified the input RF energy. Using TiN as metal gate in DG-MOSFETs the output rectified voltage increased 0.15 V, compared with the obtained with conventional N-MOSFETs. Finally, just two stages are necessary to achieve the optimal performance of rectifier; less than with conventional N-MOSFETs.

SCEs have been added and now the model supports long and short channel device.

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