A Low-Power Fully Integrated CMOS RF Front-End Receiver for 2.4-GHz-band IEEE 802.15.4 Standard

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Abstract— **This paper presents a low power 2.4 GHz front-end receiver for 2.4-GHz-band IEEE 802.15.4 standard in 0.18 µm CMOS technology. This front-end receiver adopts a low-IF architecture and comprises a variable gain single-ended low-noise amplifier (LNA), a quadrature passive mixer and a variable gain transimpedance amplifier (TIA). The front-end receiver achieves 42.7 dB voltage conversion gain, 12 dB noise figure (NF), 34 dBc image rejection and 2.5 dBm input third-order intercept point (IIP3). It only consumes 4.334 mW.**

Keywords-component; : RF front end, CMOS RFIC, IEEE 802.15.4 receiver, low-noise amplifier (LNA), passive quadrature mixer,

I. INTRODUCTION

The last decade has seen the rise of CMOS as the choice technology in consumer-based wireless applications. Full system integration continues to be a topic of interest in this research field in order to minimize both the cost and the form-factor of wireless transceivers. In the interests of longer battery life, ultra-low power design has recently become a hot topic for applications such as wireless personal area networks (WPAN), and wireless sensor nodes. The IEEE 802.15.4 standard has been specifically designed to cater to this demand. This standard operates in the 868 MHz/915 MHz/2.4 GHz Industrial, Scientific and Medical (ISM) bands with a data rate varying from 20 to 250 kb/s depending on the operating frequency band.

This paper describes the design and implementation of a low-power fully integrated CMOS RF front-end receiver for 2.4-GHz-band IEEE 802.15.4 standard. The front-end receiver architecture is discussed in Section II. Section III summarizes the simulation results of the implemented front-end receiver and, finally, some conclusions are given in Section IV.

II. FRONT-END RECEIVER ARCHITECHTURE

Direct conversion architectures (Zero-IF and Low-IF) are widely used to implement radios in a single chip. The low-IF architecture does not exhibit either a severe dc offset or 1/f noise, although it has the drawback of a restricted image rejection, which can be accomplished by a complex filter. However, the requirements of the image rejection filter are very relaxed in the IEEE 802.15.4 Standard, which is the reason why a number of IEEE 802.15.4 receivers in the literature use a low-IF receiver architecture[1]-[4].

The front-end receiver architecture is introduced in Figure 2. An inductive degenerated cascode LNA topology is used at the input. This topology is known to provide high gain, low noise and high input/output isolation. In order to achieve simultaneously low noise and input matching, the inductive degeneration technique is used.

A passive double-balanced downconversion mixer has been chosen because it dissipates no dc current, provides high linearity and reduces the LO leakage. Also, as no dc current flows through the transistors, the *1/f* noise contribution from the mixers is minimized.

The current signal from the mixer is converted to voltage by a TIA. This amplifier consists of two inverters in parallel and resistive feedback loops.

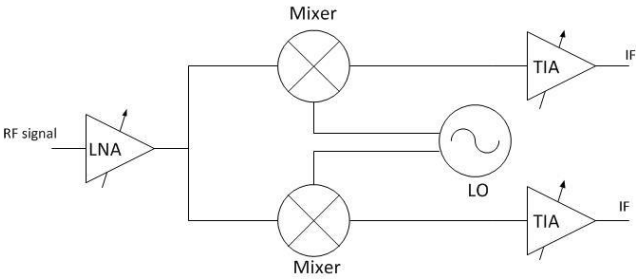

Figure 1. System architecture of the proposed front-end receiver.

The front-end receiver layout, shown in Figure 3, was done with Virtuoso software, from Cadence, using UMC 0.18 µm CMOS technology.

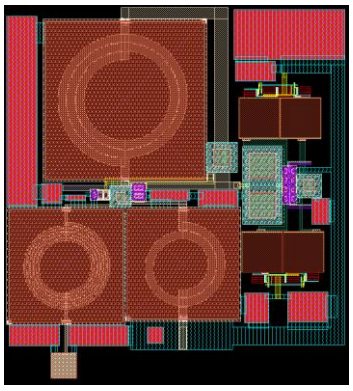

Figure 2. Layout of the proposed front-end receiver.

III. Simulation Results

The proposed front-end receiver was simulated using Advanced Design System (ADS) software. A complex filter was added in order to perform the simulations. The total power consumption of the receiver is 4.334 mW – 1.70 mA at 1.8V for the LNA, 60 µA at 1.4 V for the mixer&TIA, and 0.85 mA at 1.4 V for the complex filter.

The gain and NF (both schematic and post-layout simulation) for the entire IEEE 802.15.4 standard band are shown in Figure 3. The noise figure varies from 10.3 dB to 12 dB over the whole band while the gain varies from 44.7 to 43 dB in schematic simulation. In post-layout simulation there is a 2 dB decrease in gain and a 1.8 dB increase in NF due to metal parasitic resistance and capacitance.

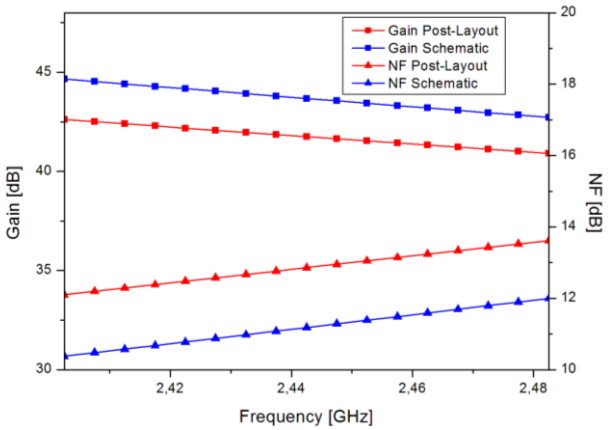

Figure 3. Simulated Gain and NF of the receiver over the entire ISM-band.

The simulated value of the receiver's NF for one channel is shown in Figure 5. The simulation shows a constant value of 10.3 dB approximately in schematic simulation, with a high rise at low frequencies due to the 1/f noise. The post-layout simulation shows an increase of approximately 1.8 dB.

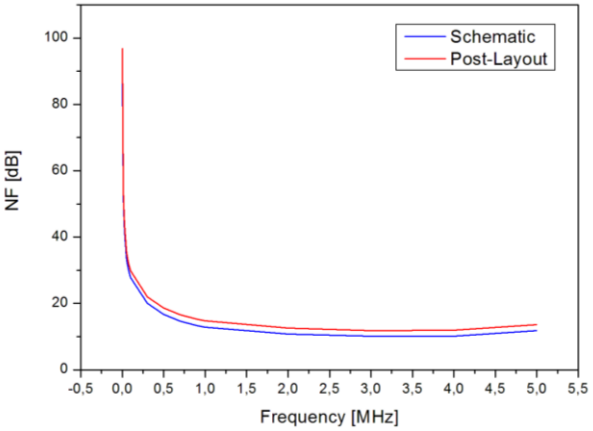

Figure 4. Simulated NF of the receiver.

In Table I, the post-layout total gain and NF of the receiver, are shown depending on the gains of the LNA and the TIA. The total gain can be varied from 3.8 to 42.7 dB while the NF changes between 12 and 45 dB.

Table I Receiver Gain and Noise Figure for different gain setups

LNA gain [dB]	TIA gain [dB]	Receiver Gain [dB]	Receiver NF [dB]
2.6	1	3.8	45
17.2	1	19	30
2.6	24	27.4	26.7
17.2	24	42.7	12

Finally, Table II compares the proposed receiver to previously reported IEEE 802.15.4 receivers. It shows that our results are in line with the state-of-the-art of low-power/low-cost front-end receivers.

Table II Performance Comparison of 2.4 GHz IEEE 802.15.4 Receivers

	[1]	[2]	[3]	[4]	This Work
Technology CMOS [nm]	180	180	90	180	180
Voltage Gain [dB]	86	30	67	-	42.7
NF [dB]	8.5	7.3	16	<10	12
IIP3 [dB]	-8	-8	-10.5	>-15	2.5
Power dissipation [mW]	12.63	6.3	10	10.8	4.334
Architecture	Low-IF: LNA+MIX +FIL+PGA	Low-IF: LNA+MIX	Low-IF: LNA+MIX +FIL+PGA	Low-IF: LNA+ MIX+ FIL+PGA	Low-IF: LNA+ MIX +FIL

LNA: Low Noise Amplifier
MIX: Mixer
FIL: Complex Filter
PGA: Programmable Gain Amplifier

IV. Conclusions

This paper presents the design of a low-power fully integrated CMOS RF front-end receiver for 2.4 GHz-band IEEE 802.15.4 Standard. Both schematic and post-layout simulations show that the achieved performance exceeds the requirements of 802.15.4, yet performs favorably in terms of high level of integration and low power consumption.

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