A Low-Power Fully Integrated CMOS Complex filter for 2.4-GHz-band IEEE 802.15.4 Standard

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Abstract— **This paper presents a low power complex filter for the 2.4-GHz-band IEEE 802.15.4 standard in 0.18 µm CMOS technology. The designed complex filter is based on Nauta's and class A-B's transconductors in order to minimize the power consumption. The circuit achieves an image rejection of 34 dB, meeting the standard's requirements. This results are accomplished with a power consumption of only 1.18mW.**

Keywords-component; : RF, CMOS RFIC, IEEE 802.15.4 receiver, OTA, gm-C

I. INTRODUCTION

The last decade has seen the rise of CMOS as the choice technology in consumer-based wireless applications. Full system integration continues to be a topic of interest in this research field in order to minimize both the cost and the form-factor of wireless transceivers. In the interests of longer battery life, ultra-low power design has recently become a hot topic for applications such as wireless personal area networks (WPAN), and wireless sensor nodes. The IEEE 802.15.4 standard has been specifically designed to cater to this demand. This standard operates in the 868 MHz/915 MHz/2.4 GHz Industrial, Scientific and Medical (ISM) bands with a data rate varying from 20 to 250 kb/s depending on the operating frequency band.

This paper describes the design and implementation of a low-power fully integrated CMOS complex filter for 2.4-GHz-band IEEE 802.15.4 standard. The complex filter architecture is discussed in Section II. Section III summarizes the simulation results of the implemented circuit and, finally, some conclusions are given in Section IV.

II. COMPLEX FILTER ARCHITECHTURE

The IEEE 802.15.4 standard requires 0 dBc rejection at the adjacent channel (5 MHz) and 30 dBc rejection at the alternate channel (10 MHz), as it can be seen in Figure 1. This can be accomplished by a Butterworth third order gm-C complex filter. The main advantage of this topology is that the inherent insertion loss of passive filters can be compensated by the transconductance of the input stage. Also, a good trade-off in terms of power, operating frequency and noise can be achieved [1][2].

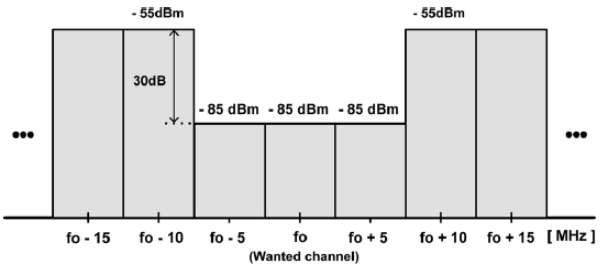

Figure 1. Blocking profile in the 2.4-GHz band for Zigbee radio

The topology of the complex filter is shown in Figure 3. It consists of two Butterworth third order gm-C low-pass filters for the I and Q paths and two crossing extra signal paths per integrator to transform the low-pass prototypes to their band-pass complex counterparts.

In order to reduce the power consumption, inverter based transconductors have been used in the I and Q paths (Figure 2.b). The main issue with this kind of transconductors is the difficulty of setting the dc levels. To maintain the output common mode voltage stability, Nautas' transconductors (Figure 2.a) have been used in the crossing signal paths that connect the I and Q branches [3]. In this type of transconductors, inverters Inv3, Inv4, inv5 and Inv6 are used to maintain common-mode stability and enhance dc gain. Common-mode stability follows if the common-mode gain (ACM) is less than unity. On the other hand, if the width of the transistors in Inv4 and Inv5 are designed slightly smaller than those of Inv3 and Inv6 the differential mode gain (ADM) is boosted [4].

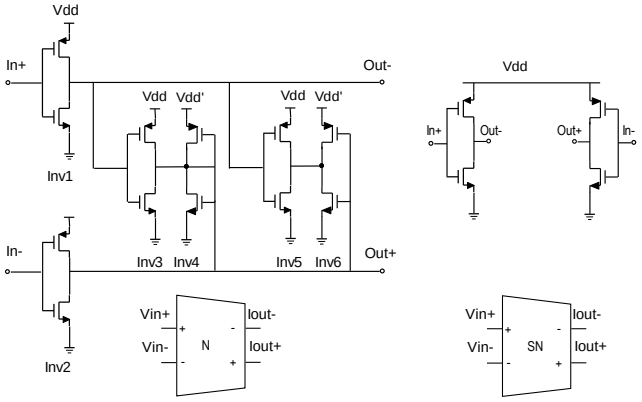

Figure 2. (a) Nauta's Transconductor (b) Simplified Nauta's transconductor

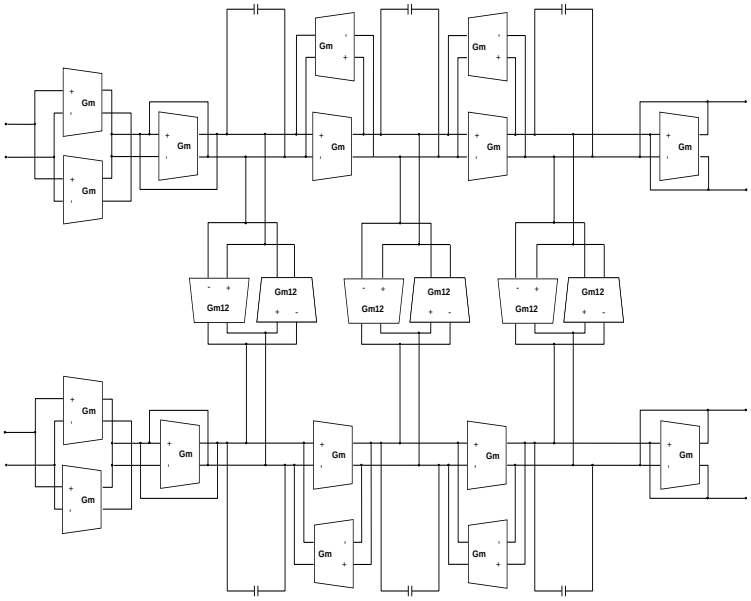

Figure 3. Schematic of the complex filter.

The complex filter layout, shown in Figure 4, was done with Virtuoso software, from Cadence, using UMC 0.18 µm CMOS technology.

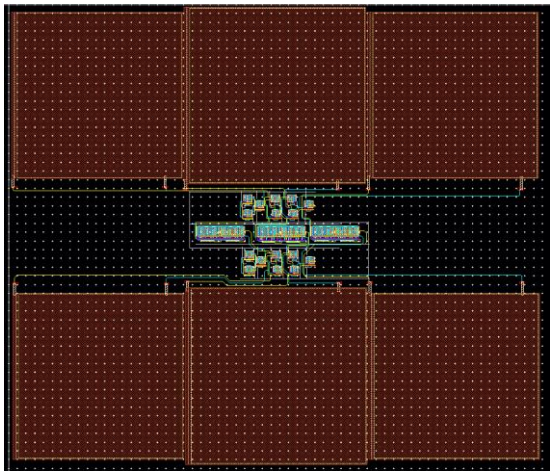

Figure 4. Layout of the proposed complex filter.

III. Simulation Results

The proposed complex filter was simulated using Advanced Design System (ADS) software. The total power consumption of the circuit is only 1.18mW.

The frequency response of this filter is shown in Figure 5. As a consequence of both dispersions in the process of fabrication and variations of the voltage power supply, this frequency response may suffer variations. These deviations can be compensated by controlling the voltage supply of the transconductors with a tuning circuit that controls the voltage supply of the complex filter transconductors. In the Nautas' transconductors the voltages Vdd and Vdd' are used for F-tuning and Q-tuning, respectively.

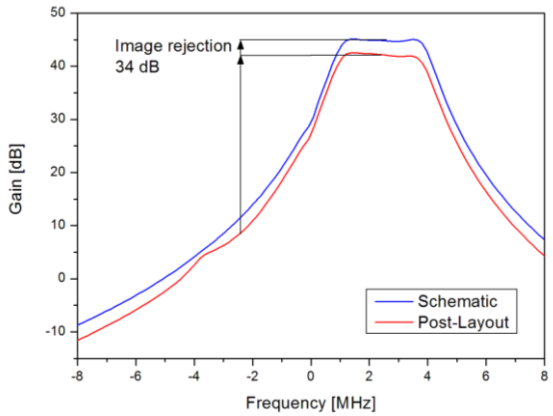

Figure 5. Frequency Response

IV. Conclusions

This paper presents the design of a low-power fully integrated CMOS complex filter for the 2.4 GHz-band IEEE 802.15.4 Standard. Both schematic and post-layout simulations show that the achieved performance exceeds the requirement of 802.15.4, which is 20 dBc of image rejection.

References

[1] Brian Guthrie, John Hughes, Tony Sayers ,and Adrian Spencer, "A CMOS Gyrator Low-IF Filter for a Dual-Mode Bluetooth/ZigBee," IEEE Journal of Solid-State Circuits, vol.40, no. 9, Sep. 2005.

[2] Trinidad Sánchez-Rodríguez, Ramón G. Carvajal, Sunil Lalchand Khemchandani, Javier Del Pino, Jaime Ramírez-Angulo, and Antonio López-Martín, "Low-Power Complex Filter for WLAN Applications," XXII Conference on Design of Circuits and Integrated Systems.

[3] Bram Nauta, "A CMOS Transconductance-C Filter Technique for Very High Frequencies," IEEE Journal of Solid-State Circuits, vol.27, no.2, Feb 1992.

[4] Carlos Muñiz-Montero, Ramón González-Carvajal, and Alejandro Díaz-Sánchez, "A Nauta's transconductor with continous-time offset compensation," Conference